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Abstract:	This document describes the status of the construction of the Version 1 of the Neuromorphic Computing Platform after the first Project year, as of Project Month 12)
Keywords:	NM-PM1, NM-MC1, Neuromorphic Computing Platform

Document Status

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3.7	1 December		Milestone info added

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1. Introduction

1.1 The Human Brain Project (HBP)

The Human Brain Project (HBP) is a major international scientific research project, involving over 100 academic and corporate entities in more than 20 countries. Funded by the European Commission (EC), the ten-year, EUR 1 billion project was launched in 2013 with the goal "to build a completely new ICT infrastructure for neuroscience, and for brain-related research in medicine and computing, catalysing a global collaborative effort to understand the human brain and its diseases and ultimately to emulate its computational capabilities."

The fields of neuroscience, medicine and information technology each have important roles to play in addressing this challenge, but the knowledge and data that each is generating have been very fragmented. The HBP is driving integration of these different contributions.

During the Ramp-Up Phase, the HBP will collect strategic data, develop theoretical frameworks, and perform technical work necessary for the development of six Information and Communication Technology (ICT) Platforms during the Operational Phase. The ICT Platforms, offering services to neuroscientists, clinical researchers and technology developers, comprise Neuroinformatics (a data repository, including brain atlases and analysing tools); Brain Simulation (building ICT models and multi-scale simulations of brains and brain components); Medical Informatics (bringing together information on brain diseases); Neuromorphic Computing (ICT which mimics the functioning of the brain); and Neurorobotics (allowing testing of brain models and simulations in virtual environments). A High Performance Computing Platform will support these Platforms.

1.2 HBP Subproject 9: Neuromorphic Computing Platform

This section summarises key features of the HBP's Neuromorphic Computing Platform

Complementarity: The Platform provides access to two different and complementary neuromorphic computing technologies. The mixed-signal PM (physical model) system currently consists of 4 million analogue neurons and 1 billion synapses, which are implemented on 20 8-inch silicon wafers. Biological and electronic parameters of the cells, as well as the network topology, are user-configurable. The biological model for the neurons is the Adaptive-Exponential-Integrate-and-Fire Model (AdEx). Synapses have 4-bit precision weights and feature short-term and long-term plasticity. The system is accelerated and runs at 10,000 times biological real-time. The digital MC (many-core) system initially consists of 500,000 ARM968 processor cores. A single chip contains 18 cores running integer arithmetic at 200 MHz, a shared system RAM and a router for address and package-based spike transmission. Each chip has 6 bi-directional links capable of transmitting 6 million spikes per second. A 128-megabyte DRAM is stacked on the chip die. The system runs at biological real-time.

Configurability: In view of the exploratory phase of neuromorphic computing, it is essential that the systems under construction are as unconstrained as possible, given the chosen technological approaches. Both HBP systems offer a very high degree of configurability with respect to the network architecture and the local models used for neurons, synapses and plasticity.

The PM system uses cross-bar switches, analogue floating gates and SRAM cells for this purpose. The MC system is based on programmable ARM cores connected by bi-directional links. Both systems are capable of performing a wide range of experiments ranging from biological reverse-engineered circuits to highly abstract networks, which may be as extreme as random connectivity.

Low Energy and High Speed: Both HBP NM systems offer advantages that surpass traditional simulation computers by several orders of magnitude in terms of their energy consumption and simulations time. The energy gap in performing a single synaptic transmission between the biological brain and a detailed computer simulation is as large as 14 orders of magnitude, corresponding to 10 fJ

in the former case and 1J in the latter. Simplified models executed on traditional computers lead to a reduction to 0.1 mJ, which is still 10 orders of magnitude worse than biology. The HBP's NM systems consume 10,000 pJ and 100 pJ for the MC and the PM systems, respectively. These numbers are not obtained from isolated lab samples, but rather from fully functional systems including all overheads from control systems, losses in power supplies and similar effects.

Simulations of large networks on traditional computers typically run 100 to 1,000 times slower than biological real-time. This renders a real-time link to physical robots or a study of slow learning and developmental processes impossible. In this respect, the complementarity of the two HBP systems is very evident. The MC system operates at biological real-time, making it an ideal candidate to connect to physical robots with vision and sound sensors as well as mechanical moving parts and actuators. The PM system, with the large acceleration factor of 10,000, can compress a day of development into 10 seconds. This provides the only known access to slow learning and developmental processes with an effective biological timing precision in the sub-millisecond regime, where processes like STDP drive the dynamics of synapses. The large acceleration factor even allows the exploration of evolutionary time-scales in experiments lasting several days or even months.

Scalability: The scale of both Phase 1 systems is entirely determined by the funds available for their construction. For growth of up to a factor 10, the cost for larger systems will simply scale with the growth factor, and no fundamentally new technological approaches would have to be developed. This is an important feature of the massively parallel approach, and it should be exploited whenever extra funding becomes available. For even larger systems, the costs will start to grow faster than linear because of costs for more advanced infrastructure like space, power and cooling. Also, new assembly technologies like 3D-integration and automated manufacturing would drive the costs. At this point, upgradability will become an important feature (see below).

Hybrid Operation: Although there are early experiments that need to be performed with stand-alone neuromorphic systems, the important new insights will only arise once those systems interact with data or the environment, and once learning and development are driven by those interactions. In the case of the real-time MC system, closed external perception-action loops can be implemented using physical robots. For the accelerated PM system, this is not feasible. Here, the external data will be provided by a nearby high performance computer operating in a closed loop with the NM system. This so-called hybrid operation of an NM system with a traditional computer is also required for other purposes, like functional simulations of larger brain areas for a multi-scale approach, or for performing the mapping and routing of reverse-engineered biological networks to the hardware substrate. For this reason, the PM system will operate a 5-teraflop machine in close physical proximity to the NM system.

Non-Expert User Access: The application of NM systems has so far been restricted to users with very detailed knowledge about the specific underlying hardware system and the dedicated software package provided to operate the system. This is very different from traditional computers, where established software packages allow efficient use with very little training effort. The HBP NM Platform systems will provide a unified software suite that enables access by non-expert users. A typical example is neuroscientists running experiments implementing reverse engineered circuits. The software suite contains a description language for networks (PyNN), the mapping and routing from biology or a theoretical model to the hardware substrate, a simulation and verification tool, and tools for the storage and the analysis of the produced data. The NM software suite will be integrated into the HBP Unified Portal, allowing for integration with the Neuroinformatics Platform, the brain simulations and the neurorobotics simulation environment.

Upgradability: Data integration and simulation in the HBP are expected to deliver a clearer idea of which aspects of neural circuits are essential for computation. This new knowledge will most likely require the design of new and improved electronic circuits, including the necessary new chip design. Also, device and VLSI technologies will develop and more advanced process nodes are likely to become accessible to neuromorphic computing. The groups in SP9 are therefore already developing concrete plans to upgrade their systems. In this context, "upgradability" is very important. Infrastructure

elements like power supplies, cooling, racks, control boards, readout- and monitoring systems, and the software tools will be transferred to and reused by the new hardware generations in order to reduce the development time.

1.3 Purpose of this Document

This report will describe progress in the development of the Neuromorphic Computing Platform, and related software tools. The document refers frequently to the M6 specification document Deliverable D9.7.1[1].

1.4 Structure of this Document

The remainder of this document provides an SP-level overview, highlighting the SP's main accomplishments and issues in M1-M12, as well as accomplishments and issues within individual components of the SP.

- WP9.1: Neuromorphic Computing with Physical Emulation of Brain Models
- WP9.2: Neuromorphic Computing with Many-core Emulation of Brain Models
- WP9.3: Software Tools for Neuromorphic Computing (Benchmarks)
- WP9.4: Novel Technologies for Neuromorphic Circuits
- WP9.5: Neuromorphic Computing Platform: integration and operations
- WP9.6: Neuromorphic Computing Platform: user support and community building
- WP9.7: Scientific Coordination

The Annexes present in tabular form what the Subproject planned to achieve in this period and what it actually achieved, including the Subproject's Scientific Key Performance Indicators (SKPIs).

1.5 Overview of Subproject 9 Achievements

We wish to begin this report with a general comment concerning the relationship between the HBP and the predecessor projects, SpiNNaker and BrainScaleS. Both HBP Phase-1 systems (NM-MC-1 and NM-PM-1) use the technology of predecessor projects. This concerns chips, printed circuit boards and a major part of the firmware and software to operate them. Within the HBP, the predecessor systems are scaled to the sizes of 500,000 processors and 20 wafers, respectively. Delays and production problems in the predecessor projects consequently affect the large-scale HBP systems.

In the HBP's first year, Subproject 9 worked on three major lines of research:

1. Construction of the two complementary neuromorphic computing systems, NM-PM-1 and NM-MC-1
2. Set-up of the unified software workflow to operate the two systems

[1] The code of the TeX document is in the repository https://brainscales-r.kip.uni-heidelberg.de/projects/hbp-sp9-specification--d9-7-1 An automatic build job https://brainscales-r.kip.uni-heidelberg.de: 8443/view/doc/job/doc_HBP-spec/ creates the a standalone .pdf document from it. An exported public version of the document (with confidential NM-PM1 material removed) is accessible at https://flagship.kip.uni-heidelberg.de/jss/SU/p/HBP_SP9_D9.7.1_NeuromorphicPlatformSpec_public.pdf

3. Preparation of the next-generation neuromorphic chips that will be used in the follow-up systems NM-PM-2 and NM-MC-2, to be constructed after the Ramp-Up Phase is completed

The primary resources supporting the upscaling of SpiNNaker hardware to the NM-MC1 are not from the HBP. This work is funded by the EPSRC (UK government-funded) project, and an additional contribution from the University of Manchester. HBP funds the upscaling of the support software to allow the full machine to be used through the HBP Portal. We had working small-scale software as the baseline at the start of the HBP, but the software has been fully refactored within the HBP to support he upscaling.

The upscaling of the BrainScaleS system to the NM-PM1 system is supported by HBP, but all basic hardware and software development for the wafer system are carried out in Work Package 3 of the BrainScaleS project, and its related deliverables. Both upscaled HBP systems will be delivered during the second HBP Project year. The first year was fully dedicated to hardware construction and development of Platform-related software.

In general, the construction of both systems has progressed well. For the PM system, all printed circuits boards have been designed and a complete prototype system has been assembled in hardware. The rack, power and cooling infrastructure has been prepared and is waiting for the installation of 20 wafer modules. For the MC system, a complete rack with 100,000 ARM cores has been assembled and is now being tested.

The development of a unified software framework demonstrated basic functionality during the HBP Summit in September 2014. Both systems in Heidelberg and Manchester have been accessed through a common software framework, and have reported their results back to the users. This is a major achievement, because so far, no neuromorphic computing system worldwide has ever been able to offer this kind of seamless service to non-expert users. As an additional area of software development, SP9 has started to collect a set of benchmark computing tasks that can be used to quantify performance of neuromorphic computing and relate it to traditional supercomputing approaches.

In parallel with substantial efforts to construct the first HBP systems, preparations for the Phase 2 versions have progressed very well. Under the leadership of the Manchester group for the MC system and the Heidelberg group for the PM system, prototype chips have been designed and will be sent to manufacturers soon. This work catalysed thorough integration among the Subproject partners. A significant fraction of the partner groups are involved in work on the chips—the new many-core and the new analogue chip. This is an important development, because the current systems are still based on the circuit concepts developed in the SpiNNaker and BrainScaleS projects.

1.6 Overview of Subproject 9 Problems

The construction of the PM system requires design, manufacturing, testing and installation of 2,500 printed circuit boards. This is a very large undertaking, which is due to finish in Month 18. A major problem has been the manufacturing of the main board for NM-PM-1 by industry partners. Two independent manufacturers have been working to produce prototypes. One has not succeeded, and the other has experienced major delays[2]. The contract has now been awarded to the second company, but a delay of approximately six months is to be expected because serial manufacturing will only start around Month 13. This may lead to a delay of the complete system of about the same time, effectively pushing the completion date back of the whole system to Month 24 rather than Month 18 (main boards will arrive in lots and be used to assemble systems as they arrive, so systems will become available before the boards for constructing all 20 are available). In view of the size of the Project and the

[2] See section 6.3.1 for additional information.

limited funding for engineering support, this delay seems acceptable and we will still deliver the complete system by the end of the HBP Ramp-Up Phase.

1.7 The Next Six Months for Subproject 9

The next six months will be mostly dedicated to system construction. Both systems (MC and PM) will have to produce all their printed circuit boards and start assembly. Month 18 is the delivery date for both hardware systems, and commissioning will start thereafter. As described in the previous paragraph, as six-month delay has to be expected for the complete PM system. On the software side, the integration of the Neuromorphic Platform access into the HBP-wide Unified Portal will be the major line of activity. Both system approaches will involve submitting next generation neuromorphic chips for production, and evaluating their performance.

The validation of SpiNNaker hardware is a progressive process from wafer test, through package test to PCB test, and finally system test and commissioning. The validation of the software is based on running example networks of increasing size through the tools, and comparing the results with a reference software simulator such as NEST. Some of the larger example networks have been developed in collaboration with HBP Partners, for example the Diesmann cortical microcolumn model and the KTH BCPNN model.

2. Neuromorphic Computing with Physical Emulation of Brain Models (WP9.1)

2.1 Neuromorphic Computing with Physical Emulation of Brain Models: Overall Goals

The part of the SP9 Platform implementing "Neuromorphic Computing with Physical Emulation of Brain Models" is based on a hardware system called the Neuromorphic Physical Model (NM-PM). It consists of a custom hardware system that implements the physical emulation of brain models, and a conventional compute cluster to interface the custom part with the user, and to execute parts of the model in synchrony with the physical models. These hybrid models are essential for all tasks involving motor feedback to the environment, since the physical model is limited to modelling neurons and synapses. This WP also prepares the NM-PM2 system (development of new VLSI circuits and implementation in test chips).

WP9.1 comprises the following Tasks:

- T9.1.1 Development and implementation of VLSI circuits emulating neurons and synapses
- T9.1.2 Development and implementation of high density configurable VLSI spike communication networks
- T9.1.3 Development and Implementation of neuromorphic systems-on-chip (SOCs)
- T9.1.4 Integration of the neuromorphic SOCs into the NCS framework
- T9.1.5 Development of low level software and firmware for the neuromorphic system

2.2 Neuromorphic Computing with Physical Emulation of Brain Models: Main Achievements

2.2.1 T9.1.1

Many novel circuits have been developed for the accelerated analogue neuromorphic hardware. Enhanced versions of the synapse and neuron circuits have been implemented in a 65nm low-power process technology. The novel synapse circuit has a reduced leakage and offset. The resolution was also increased from 4 to 6 bit, while the correlation measurement for the plasticity circuits feature better tracking of causal and anti-causal parts and a vastly increased range of usable time-constants.

A novel synaptic input circuit for the neuron has been developed that realizes an enhanced dynamic range and improved linearity. The neuron uses a multitude of bias currents and voltages to adjust its parameters to the desired operating point. In the PM1 neuromorphic system, these parameters were stored on analogue floating gate memory cells. Since these cells proved to be difficult to control precisely, we decided to remove them in the new PM2 system and replace them with a more robust capacitive analogue memory with built-in SRAM refresh. We adapted a capacitive parameter memory circuit to the novel neuron circuit.

For enhanced plasticity features, we developed a novel concept using a combination of analogue correlation measurements and digital weight calculations. A custom plasticity-processing unit using a highly parallel SIMD-ALU tailored for weight update processing has been developed for this purpose. A column-parallel ADC has been developed to convert the analogue correlation data from the synapses into digital data for the plasticity-processing unit. All said circuits have been integrated within a prototype ASIC, which will be manufactured during Q4/14. The prototype resembles a small network chip with 64 neurons and 2,048 synapses.

2.2.2 T9.1.2

We have developed a novel SerDes-IO circuit and implemented it in 65nm technology. It is compatible with the physical level of the existing PM1 neuromorphic system, but features improved testability and improved SNR. A prototype ASIC has been developed and sent for manufacturing[3].

2.2.3 T9.1.3

The SoC design for NM-PM-1 has been completed, as has the design of peripheral PCBs of the Wafer Module (PowerIt, AuxPwr, Cure, AnaB). Prototypes are currently being or have been tested. Power supply PCBs (PowerIt, AuxPwr) are tested with an electronic load, first. Passing this synthetic full-load test qualifies for load testing with the wafer module. After passing these tests, the power supply boards are qualified for being mounted to the Wafer Module. Reticle control boards (Cure) and analogue readout units are tested and calibrated (slope and offset of ADC preamplifiers) with dedicated test stands. All tests are documented in Wikis that are part of the respective design repository. Relevant calibration data are stored in the NM-PM-1 calibration framework.

2.2.4 T9.1.4

The FPGA communication PCB (FCP) has been designed and successfully tested. The FCP firmware is developed in VHDL and VERILOG. The source code is maintained in a repository[4]. For synthesis, place-and-route and simulation, we are using a design flow that has been provided by partner TUD. It employs Xilinx software for the design implementation and Cadence software for simulation. The main simulation environment is a system-level testbench. For crucial components like the communication link layer (ARQ), unit tests have been developed (test-driven design). The documentation of the functionality and interfaces is available in D9.7.1. Regarding bandwidths, wire-speed performance is reached for the host interface as well as the wafer interfaces.

A first set of 54 FCPs has been manufactured for the BrainScaleS system, sufficient for the equipment of one wafer module (48 for one system). The design of the Wafer IO boards has been completed and a first set of 4 vertical IO boards and 4 horizontal IO boards has been sent for manufacturing. For one system, 2 vertical and 2 horizontal boards are required. 40 boards each are required for 20 systems.

2.2.5 T9.1.5

FPGA firmware modules for all interfaces have been developed. FPGA firmware and software were implemented for fully automatic testing of all FCP components and communication links. Tests for all manufactured FCPs were successfully completed.

Over the last few months, an ARQ-based Host-FCP transport-layer protocol has been implemented. Extensive performance and reliability tests show adequate performance for interconnecting wafer modules and cluster control nodes. Tests performed on the first wafer prototype system show almost linear scaling up to 8 FPGAs (which is the maximum number on this prototype). Integration tests that cover all communication links and FPGA functionality will be performed as soon as possible.

Basic playback memory functionality has been implemented, tested and integrated into the software stack. Other changes relating to AnaRM and FCP allow for synchronised experiment runtime and recording of analogue membrane data. All work affecting the FCP has been carried out in close collaboration with TUD and UHEI. The components are described in the SP9 specification document (Deliverable 9.7.1).

[3] Repository: https://brainscales-r.kip.uni-heidelberg.de/projects/hicann-dls
[4] https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga

2.3 Neuromorphic Computing with Physical Emulation of Brain Models: Main Problems

2.3.1 T9.1.5

Generally, integration of independently developed FPGA units is non-trivial, and extensive and automated testing is key to success. Unit tests thus far do not cover all software and firmware modules. Existing automated integrated tests using the complete chain do not completely cover the communication stack. Thus, the communication stack between host and wafer electronics is not yet completely stable, and errors are sometimes hard to find. New test cases are created when a bug is found, or when new functionality/operation modes are tested for the first time. Writing tests is a key component of software development.

2.4 Neuromorphic Computing with Physical Emulation of Brain Models: The Next 6 Months

2.4.1 T9.1.1

The manufactured prototype ASIC will be thoroughly tested, and development will continue based on the results from the prototype. A test setup for the laboratory will be developed and manufactured, including a test PCB and FPGA firmware for the existing FPGA-based test platform. Tests include verifying correct operation of the novel synapse and neuron circuits and running test software on the build-in plasticity unit. Further tests, like setting up a complete network circuit and testing the complete plasticity loop, will most likely only take place after the next 6 months.

2.4.2 T9.1.2

The manufactured prototype ASIC will be thoroughly tested, and development will continue based on the results from the prototype (see section 2.4.1). In addition, the 65nm implementation of the high-speed on-wafer communication circuits will continue. A circuit approach based on a digital PLL to replace the current analogue DLL-circuit will be evaluated in the next 6 months.

2.4.3 T9.1.3

During operation of the current wafer modules, it turned out that input calibration circuitry of the analogue front-end boards (AnaFP) could be improved. However, since the analogue quality is sufficient for experiment operation, the AnaFP design will be used as-is for the analogue readout modules (AnaRM) that will be used for M18 (60 boards have been produced, which need to be assembled and tested). A re-design during the next six months is an option (this has not yet been decided).

2.4.4 T9.1.4

All development for this Task that is relevant for the M18 system has been completed. Production of all components will be organised and reported in Task 9.5.1

2.4.5 T9.1.5

FPGA interface modules and Host-ARQ will be integrated into a firmware top-level for wafer operation, porting and adapting core components from existing designs. The robust operation of the system has to be verified, and remaining issues that reduce availability/uptime or require manual interaction need to be identified and solved. This will mostly rely on broad test coverage in simulation and on hardware. The latter is also related to automatic testing of software changes that are developed within T9.5.4.

Additional features will address support for precise experiment timing of both, spike input and configuration data. Other changes will be related to closed-loop experiment support. The closed-loop operation mode is described in the PhD thesis of Eric Müller[5].

[5] https://www.kip.uni-heidelberg.de/Veroeffentlichungen/details.php?id=3112

3. Neuromorphic Computing with Many-core Emulation of Brain Models (WP9.2)

3.1 Neuromorphic Computing with Many-Core Emulation of Brain Models: Overall Goals

The Neuromorphic Multi-Core Platforms (NM-MC1, NM-MC2) provide cheap, reliable, and readily available platforms on which to perform experiments for the Human Brain Project. Currently, these experiments are expected to fall into two broad areas: those supporting the neuromorphic approach to brain modelling (i.e., reduced cortical circuits using point neurons and neurorobotics experiments); and those exploring features used in the Simulation Platform (i.e., virtual environments with performance that can be explored before the Simulation Platform is ready).

The flexibility of the digital approach to neuromorphics means that if other suitable experiments are required, then this is just a matter of re-programming stock microprocessors. The Neuromorphic Multi-Core Platform will leverage prior investment by the UK Engineering and Physical Science Research Council (EPSRC) in SpiNNaker technology to provide a half million-core machine suitable for brain simulation. The basis of the system is a novel 18-core chip. This component can be incorporated into larger systems because it has built-in inter-chip communications. The full 500,000-core machine has a total memory capacity of 4 terabytes, and at most, 600 100-megabit ethernet connections. We envisage that these data will not be directly loaded or written back to the backing store. Instead, a description of the data will be loaded, which will then be expanded on the NM-MC1 system using the full 500,000 cores. For check-pointing purposes, we currently envisage writing back deltas on the original data sets. This approach is subject to change, should alternatives present themselves. The SpiNNaker Group at Manchester have been holding successful SpiNNaker Workshops, and these will continue, in part funded by the HBP grant. So far there, have been three Workshops with 20 attendees per workshop, and a fourth is to be held in April 2015.

WP9.2 comprises the following Tasks:

- T9.2.1 Design and implementation of digital many-core processor systems for neuromorphic computation
- T9.2.2 Design and implementation of digital networks for communication between neurons
- T9.2.3 Integration
- T9.2.4 Programming models for digital many-core neuromorphic systems

3.2 Neuromorphic Computing with Many-Core Emulation of Brain Models: Main Achievements

The development and commissioning of the NM-MC-1 many-core Platform at UMAN (P73) is proceeding largely as planned. The hardware serial production is underway, with enough circuit boards for the 500,000-processor machine already manufactured. At the time of writing, a single card-frame machine with 20,000 processors is being tested, and some minor reliability issues are being resolved. A one-rack machine with 100,000 processors is largely complete but has not yet been commissioned. The system is documented in Deliverable D9.7.1. The support software for the machine is also progressing at UMAN, although the hardware inevitably lags somewhat.

3.3 Neuromorphic Computing with Many-core Emulation of Brain Models: Main Problems

There have been no significant problems or delays.

3.4 Neuromorphic Computing with Many-core Emulation of Brain Models: The Next Six Months

The major activities over the next six months are:

- Continue to scale up the commissioned NM-MC-1 hardware and support software.
- Complete the design of the NM-MC-2 test chip.

In the next six months, this WP will focus on the NM-MC-1 (SpiNNaker) support software with the goals of 1) establishing a stable baseline for upscaling following the code refactoring; and 2) introducing new optimisations into the code incrementally to allow it to scale up to the full system. This has to be carried out via a cycle of code, test and analyse to identify critical routines, but an early optimisation strategy is to move the detailing of synaptic data structures from the host onto the SpiNNaker machine. This will accelerate both the expansion of the data structures (by exploiting the parallelism of the SpiNNaker machine) and the loading of an application onto the machine, as the unexpanded data structures are much smaller than the fully expanded ones.

The design of the NM-MC-2 test chip is on-going. The objective is to de-risk the final chip, and to demonstrate that the major performance objectives can be met. The test chip will be a small die that incorporates a small number of processors, and a SpiNNaker-style packet router that uses high-speed serial on- and inter-chip communications, with extensive power control and management features. Resources for the upscaling of the commissioned hardware largely come from outside the HBP, but the process is reported here because the HBP service delivery depends on it.

4. Software Tools for Neuromorphic Computing (WP9.3)

4.1 Software Tools: Overall Goals

Each of the neuromorphic computing systems (NCS) described in the previous sections requires a low-level software system to operate. Further layers of software are required for:

- Describing computational models and experiments
- Mapping high-level model descriptions onto the NCS
- Simplifying more morphologically and physiologically detailed neuronal models so that they can be simulated/emulated on the NCS
- Providing remote access to the NCS, eventually through integration into the HBP Unified Portal
- Simulating the behaviour of the NCS on traditional computers so that users can test and develop models while the hardware systems are still under construction
- Integrating the Neuromorphic Computing Platform with other HBP computational resources, such as data storage, HPC systems and the Neurorobotics Platform
- Measuring the performance of the NCS, in terms of speed, energy consumption, accuracy and other metrics, through the development of benchmarks

These further layers of software are either common to all the NCS (e.g., model description software), or have considerable overlap in principles and concepts between the physical-model and many-core systems (e.g., mapping and routing, benchmarks). The provision of these higher-level software components is the goal of WP9.3.

WP9.3 comprises the following Tasks:

- T9.3.1 NCS integration with the Brain Simulation and High Performance Computing platforms
- T9.3.2 Simplifying brain models
- T9.3.3 Mapping and routing of imported circuits to the NCS
- T9.3.4 Benchmarking the neuromorphic circuits developed in WP 9.1 and WP 9.2
- T9.3.5 Executable System Specification for the neuromorphic circuits developed in WP9.1 and WP9.2.

4.2 Software Tools: Main Achievements

Milestones MS181 (Software tools specified – see D9.7.1) and MS182 (Software tools demonstrated) were achieved on time.

4.2.1 PyNN model/experiment description API

The PyNN API, and the implementations of the API for the NEST, NEURON and Brian simulators and for the NM-PM-1 and NM-MC-1 neuromorphic computing systems, originally developed during the FACETS and BrainScaleS projects, were further developed during the first 12 months, with the specific requirements of the HBP in mind.

Two beta releases of PyNN were completed. The NEURON and NEST backends have been fully updated to the 0.8 API. The update of the BrianScaleS backend is largely complete. The development branch has been updated to work with Python 3. For the NM-PM-1, PyNN implementation progressed rapidly on two fronts: 1) updating the implementation from version 0.7 of the API to version 0.8, and 2)

improving performance based on a reimplementation in C++. We undertook a major revision of the NM-MC-1 PyNN implementation to improve performance and maintainability.

The main PyNN repository, including the NEURON and NEST backends, currently contains about 28,000 lines of code (according to https://www.openhub.net/p/NeuralEnsemble-PyNN). The issue tracker reports 93 issues closed for the upcoming PyNN 0.8.0 release, with 7 issues still open. Software development follows an informal agile methodology, using the Github pull request-code review-merge workflow. The test suite contains 548 tests (unit tests + system/integration tests), which are automatically run after every commit on two continuous integration servers (https://qa.nest-initiative.org/view/PyNN/ and https://travis-ci.org/NeuralEnsemble/PyNN/).

- Software repositories:
  - Main PyNN repository: https://github.com/NeuralEnsemble/PyNN/
  - NM-PM-1 backend: git@gitviz.kip.uni-heidelberg.de:pynn-hardware.git
  - NM-MC-1 backend: https://github.com/SpiNNakerManchester/sPyNNaker
- Documentation:
  - PyNN 0.7 API: http://neuralensemble.org/trac/PyNN/wiki
  - PyNN 0.8 API: http://neuralensemble.org/docs/PyNN/
  - NM-PM-1 backend: http://neuralensemble.org/trac/PyNN/wiki/NeuromorphicHardware
  - NM-MC-1 backend: http://spinnakermanchester.github.io

4.2.2 User interface for remote access to the Platform

The user interface was fully specified during the first six months of the Project; the specification forms part of Deliverable D9.7.1. In the second six months, implementation of the user interface began, and is now progressing ahead of schedule. A minimal implementation of the common job queue service, with jobs submitted via both a web interface and a Python client and executed on both the NM-PM-1 and NM-MC-1 systems, was demonstrated at the HBP Summit in Heidelberg in September 2014. Software repository and issue tracker: https://bitbucket.org/apdavison/nmpi.

4.2.3 Interaction with HPC systems

We began to adapt the MUSIC software library for interfacing an HPC system to the NM-PM hardware. Specifically, a reorganisation of the MUSIC library was planned and partially completed, in order to abstract the communication layer and allow for UDP communication and MPI communication to co-exist.

4.2.4 Simplifying brain models

We mapped large-scale brain models to the NM-PM-1 and NM-MC-1 systems. For NM-PM-1, the Blue Brain Project (BBP) columnar network benchmark (a simplified version of the full BBP cortical column model), the Jülich Network (JuNe) model and the KTH L2/3 attractor model were successfully mapped. The fidelity of the mapping process was studied in great detail, and was described in the PhD thesis of Sebastian Jeltzsch[6], Heidelberg. The mapping code is in the repository[7].

[6] "A Scalable Workflow for a Configurable Neuromorphic Platform" http://www.ub.uni-heidelberg.de/archiv/17190

[7] Column-model: https://brainscales-r.kip.uni-heidelberg.de/projects/model-column

For NM-MC-1, the Diesmann cubic millimetre cortical circuit was implemented. The Diesmann cortical circuit mapping has been validated by comparing the SpiNNaker outputs with those of a trusted reference simulator—in this case, NEST.

4.2.5 Mapping and routing of imported circuits

Considerable work was performed on the NM-PM-1 and NM-MC-1 software for mapping and routing[8], including rewrites of the software stacks for improved performance, parallelisation and maintainability. The NMPM-1 calibration framework has been developed. Basic tasks are generating, querying, storing and applying calibration data. Methods for LIF calibration have been developed and the software stack has been integrated into the mapping layer. The calibration framework is documented in the master's thesis of Dominik Schmidt[9]. The code is in the repository[10].

4.2.6 Hardware simulation/executable system specification

The Executable System Specification (ESS) for the NM-PM-1 system, originally developed during the BrainScaleS project, was adapted to the software stack developed in T9.5.4, with significant improvements in performance, test-suite coverage, and ease of deployment. Concerning the latter aspect, two approaches were developed to provide a turn-key solution for researchers to get started with the ESS extremely rapidly: one based on the Ubuntu-Live Linux distribution, the other on the Docker Linux container technology[11]. Work was begun on a revision to the SpiNNaker Emulator (the ESS for NM-MC hardware).

4.2.7 Benchmarks

We elaborated the principles for definition of benchmarks (reference tasks and associated performance/quality measures aiming at a direct comparison of different neuromorphic and non-neuromorphic hardware systems) through a series of videoconference meetings. A working group formed that includes a representative of the Neurorobotics Platform (Marc-Oliver Gewaltig), and a version control repository was set up. A number of benchmark task descriptions have now been developed and deposited in the repository.

4.2.8 Collaboration

The work described here has involved a number of collaborations with other HBP Sub-projects, in particular SP6 (Unified Portal, NEST simulation software, model simplification), SP10 (participation in benchmark development) and the HBP visualisation team (evaluation of the MUSIC library).

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[8] NM-PM mapping: https://brainscales-r.kip.uni-heidelberg.de/projects/marocco/repository, NM-MC mapping: SpiNNaker mapping software is held in a git repository: http://github.com/SpiNNakerManchester/sPyNNaker.git (more detailed documentation will emerge as the development stabilises).

[9] "Automated Characterization of a Wafer-Scale Neuromorphic Hardware System, http://www.kip.uni-heidelberg.de/Veroeffentlichungen/details.php?id=3110

[10] https://brainscales-r.kip.uni-heidelberg.de/projects/cake/repository

[11] The ESS is available as a docker image: https://registry.hub.docker.com/u/uhei/ess-system/ The ESS source code and development is managed in: https://brainscales-r.kip.uni-heidelberg.de/projects/systemsim-stage2 FAQ and basic documentation for the ESS can be found online at neuralensemble.org http://neuralensemble.org/trac/PyNN/wiki/NeuromorphicHardware and at: http://www.kip.uni-heidelberg.de/Veroeffentlichungen/details.php?id=2003 http://www.kip.uni-heidelberg.de/Veroeffentlichungen/details.php?id=2958

4.2.9 Contributors

The principal contributors to the work described here were: Joël Chavas, Domenico Guarino, Andrew Davison (CNRS-UNIC), Eric Müller, Sebastian Jeltzsch, Christoph Koke, Sebastian Schmitt, Paul Müller (UHEI), David Lester, Andrew Rowley, Simon Davidson (UMAN), Anders Lansner, Mikael Djurfeldt (KTH).

4.3 Software Tools: Main Problems

No significant problems have been encountered. The WP is on schedule.

4.4 Software Tools: The Next 6 Months

There are no formal Milestones for WP9.3 in the next six months. Nevertheless, the activities of this Work Package will contribute to achieving Milestones MS186 (WP9.5 Internal release of the Neuromorphic Computing Platform) and MS190 (WP9.6 Guidebook for the use of the Neuromorphic Computing Platform), as well as and Deliverable D9.7.3, all anticipated in Month 18.

The main achievements expected by the end of month 18 are:

- Final release of PyNN version 0.8.0
- Completion of the preliminary user interface for the Neuromorphic Computing Platform, suitable for internal release, with execution of submitted jobs on both NCS
- Running at least four benchmark tasks on both NCS
- Preliminary internal release of ESS software
- Documentation of all systems for internal users

No changes to the original Ramp-Up Phase work plan are foreseen.

5. Novel Technologies for Neuromorphic Circuits (WP9.4)

5.1 Novel Technologies for Neuromorphic Circuits: Overall Goals

Although most of SP9's efforts during the Ramp-Up Phase will be directed to building and operating the Platform and the two NCS, the Subproject will also dedicate significant resources to the development of technologies for Phases 2 and 3. The planned work includes the development of a lamination technology to integrate silicon wafers into a layer structure of printed-circuit boards, the development of CAE tools for the design of massively parallel VLSI systems, and the evaluation of neuromorphic technologies developed outside the HBP (WP9.4).

WP9.4 comprises the following Tasks:

- T9.4.1 High density connection technologies for the integration of silicon substrates with PCB technologies
- T9.4.2 Computer aided design (CAD) methodologies for neuromorphic VLSI circuits
- T9.4.3 Functional demonstrators.

5.2 Novel Technologies for Neuromorphic Circuits: Main Achievements

Silicon monitor wafers with a thickness of 200µm have been laminated with the printed circuit board process in a stack of FR4 frame, two prepreg layers and two copper foils. The lamination was done in a heated vacuum high-pressure lamination press. We observed no cracks in the silicon wafer after the lamination, and the warpage was moderate.

The laminated copper layers have been structured by a lithography process with LDI exposure of a laminated photoresist. The copper was structured by wet etching. The inspection of the processed wafers showed no defects that indicate principal problems.

Silicon test wafers with the full rewiring layers are in the process.

The top layer was redesigned to fulfil the requirements of the PCB process. The pad size was modified to fit the alignment accuracy of the PCB process and the top layer is an electroplated copper layer with 30µm thickness to withstand the Laser drilling process to open the vias through the prepreg layer and interconnect the wafer to the board layers.

So far, three blank silicon monitor wafers have been laminated with the printed circuit board process. No mechanical defects could be observed. Electrical tests are not possible in this configuration that will be done with the test wafers, which have the full multilayer redistribution. Two of these Wafers are now ready and will be laminated soon. Five more test wafers are in the redistribution process and will be available end of the year. The next step is the laminating of the silicon test wafers in the PCB multilayer.

5.3 Novel Technologies for Neuromorphic Circuits: Main Problems

No major problems have been encountered.

6. Neuromorphic Computing Platform: Integration and Operations (WP9.5)

6.1 Integration and Operations: Overall Goals

WP9.5 comprises the following Tasks:

T9.5.1 Development of the specification for the Neuromorphic Computing System

Create a unified document describing the Neuromorphic Compute Platform on all levels, from the high-level user interface down to the microelectronic circuits. The document will contain all information necessary to assemble, maintain and operate the Platform.

T9.5.2 Neuromorphic Computing Systems – component acquisition, production and manufacturing

The NCS consists of 20 Wafer Modules (WMOD) installed in 7 server racks located at UHEI (P45). Each WMOD consists of 83 printed circuit boards (PCBs), which makes a total number of approximately 1700 PCBs. The number of mechanical components needed for each WMOD is 21. Most of these components have to be manufactured by UHEI's mechanical workshop. Only the major components are reported.

Main electrical components of the WMOD and their end numbers:

- 20 post processed HICANN Wafer
- 20 MainPCBs for the HICANN Wafer connection
- 960 FPGA based communication PCBs (FCP)
- 80 physical layer and communication connector PCBs (WIO)
- 20 main power supply PCBs (PowerIt)
- 40 auxiliary power supply PCBs (AuxPwr)
- 40 analogue breakout and system control PCBs (AnaB)
- 160 monitoring and control PCBs (Cure)
- 20 of the shelf Raspberry Pi

Mechanical parts of the WMOD:

- 20 aluminium Wafer Bracket (WBr) for mechanical fixation of the HICANN Wafer
- 20 electrosilvered Top Cover (ToCo) as a framework for the mechanical linkage of Wafer and MainPCB
- 40 Positioning Mask for the Elastomeric Stripe Connectors (PMk)
- 340 additional mechanical parts for installation of peripheral electronic components such as power supplies and system control PCBs

T5.9.3 Neuromorphic Computing Systems – assembly, operation & maintenance

The overall goal is to have 20 assembled Wafer Modules installed together with the necessary conventional compute cluster in 7 server racks. For operation and maintenance, we anticipate a contingency reserve of 10% of all necessary components.

T9.5.4 Software for Neuromorphic Computing Systems and for configuring Neuromorphic Computing Systems

T9.5.5 NM Platform website construction and maintenance

6.2 Integration and Operations: Main Achievements

6.2.1 T9.5.1

An initial version of the specification was provided in an earlier Deliverable (D9.7.1). This specification is continuously being updated and improved, and all project members always have access to the most recent version[12].

6.2.2 T9.5.2

Wafers: 25 wafers have been received by UHEI from UMC and were sent to post-processing at Fraunhofer-IZM. Three lots are currently being processed.

FCP: FPGAs and all other ICs for full assembly of NM-PM-1 have been ordered and have apart from two positions arrived at UHEI. The order for final PCB production has been placed.

System: M185: The Neuromorphic Computing Platform is fully specified in the specification document D9.7.1. The server racks hosting the Wafer Modules and the conventional compute cluster are installed with their respective cooling facilities. Prototypes of all necessary components for the Wafer Module have been produced. A fully equipped WMOD has been assembled and is currently being tested. If there are no unexpected results, the series production can begin.

Main electrical components of the WMOD and their actual status:

- Four post-processed HICANN Wafers are present at UHEI. The remaining Wafers are at the IZM for post-processing. The last batch is expected in November 2014.
- Four assembled MainPCB are present. After a positive test result, we will begin production of the remaining PCBs. The production will last until the end of 2014 and will be done in several batches. The assembling company is on standby and will start assembling when the first batch is delivered. All electrical components are already stored at the assembling company.
- 50 FPGA based communication PCBs (FCP) have been produced. The FCPs have been tested, stand-alone.
- 4 physical layer and communication connector PCBs have been produced and are currently being tested. The series production will start in Month 13.
- 5 PowerIt PCBs have been produced and tested, stand-alone. After a positive result of an integrated test the series production will take place.
- 1 AuxPwr PCB prototype has been produced and tested, stand-alone. The series production will be started in Month 13, with some minor changes.
- 1 prototype of the AnaB PCB has been produced and will have to pass an integrated test in Month 11. The series production should be complete by Month 15.
- 12 Cure PCBs have been produced and tested. They have been integrated into the WMOD and are currently used in the system. The quotes for series production are on the way, and production can begin in Month 13.
- 6 Raspberry Pi are present. The remaining pieces will be ordered in Month 13.

Mechanical parts of the WMOD:

- 10 Wafer Brackets have been manufactured. The remaining pieces are in production and are missing only some minor steps.

[12] The code of the TeX document is in the repository https://brainscales-r.kip.uni-heidelberg.de/projects/hbp-sp9-specification--d9-7-1 See footnote 1 on page 7 for more details.

- 2 electrosilvered Top Covers have been produced. One is currently used for the system integration tests. Six Top Covers are waiting for the electrosilvering process. The rest are production and will be finished in Month 14.
- 20 Positioning Masks have been produced. The production will be completed in M15.
- Prototypes of the additional mechanical parts have been produced. The series production will start in Month 13 and will last three months.

6.2.3 T9.5.3

SU (P46) has developed test-PCBs in close collaboration with UHEI for automated testing of all wafer contacts during assembly. A first prototype of the Wafer Module has been assembled, and has proven that the mechanical and electronic components all match. Meetings (in personal and via telephone conference) have taken place with SAB to develop test strategies for the series production of the Wafer Modules. First test hardware has been produced by SU.

At the end of Month 12, an assembly training for SU took place at UHEI. The aim of the workshop was to train participants on the assembly of the Wafer Modules and the different testing steps. A second adjustment facility for SU has been developed and is currently under production at UHEI's mechanical workshop.

A student assistant has been hired. He is testing the conventional hardware and is installing it together with the produced hardware into the racks.

6.2.4 T9.5.4

The software stack for automated mapping of neuronal networks described in biological terms (using the PyNN 0.7 API) to the NMPM-1 has been developed. Multiple software layers have been specified and implemented. This stack includes a hardware access layer that groups accessible hardware units together, a stateful software layer that keeps track of the hardware configuration of a given experiment, the mapping layer that produces the hardware configuration, and a user interface layer based on the PyNN API.

In the lower software layers, the primary goal is to reduce the possibility of user errors. All coordinates and data structures are strongly typed, the configuration sequence is monitored, and unsupported operation is reported to the user. The upper layers focus on user experiment. Mapping hints (e.g., for neuron placement and projection priorities) are supported as well as the acquisition of reverse mapping data. Calibration and defect data are considered in several mapping stages.

We have made first steps to update NMPM-1's PyNN API from 0.7 to 0.8 in collaboration with CNRS-UNIC. All software components have been specified in the SP9 specification, D9.7.1. The implemented software is maintained in the repository[13].

[13] https://brainscales-r.kip.uni-heidelberg.de/projects/pynn-hardware/repository/show?rev=pynn8_backend

6.3 Integration and Operations: Main Problems

6.3.1 T9.5.2

The primary cause of delays in the Wafer Module production process has been the manufacturing of the MainPCB. Due to production difficulties of the predecessor, two companies have been chosen for the manufacturing. The requirements of the system did not allow a reduction in the complexity of the board, but some changes for better producibility have been made.

Production started in January 2014. Only one company was able to deliver four faultless PCBs in M10. The production problems changed the production time of the boards from the standard six weeks to an uncertain value. This is why the series production of the boards should start as soon as possible, in order to achieve the necessary number of boards by the end of 2014.

The difficulties of the MainPCB production are caused by the size and the complexity of the PCB. Only two companies could be found that were willing to process the PCB. The high density of signals routed on the MainPCB leads to a specific layer-stack (14 layers with stacked micro vias to each layer) of the PCBs. This exceeds the standard design rules given by the manufacturer. The large size of the PCB and the increased number of processing steps shrinks the yield dramatically. One of the two contracted companies was not able to produce one error-free PCB. They produced and shipped one prototype with an undefined number of errors, and then ceased their efforts. The other company had to adapt the processing steps in order to decrease the error probability.

The high costs of the MainPCB require a thorough test of the produced prototypes, which delayed the starting of the series production.

6.3.2 T9.5.4

The main problems can be split into two classes: hardware complexity and software technological problems. Firstly, as the underlying hardware substrate is rather complex in terms of configuration and operation, the coordinate and data type system was difficult to develop and required several iterations between hardware experts/early hardware users and the developers. Secondly, ambitious software properties increased the development effort. Due to the performance requirements (mostly because of NMPM-1's high acceleration factor), all software components are written in C++. For the users, we provide an automatically generated Python wrapping and serialisable data structures between all interfaces. Looking back, the development of these "additional" features was rather complex and time-consuming. Nevertheless, except for closed-loop applications, all users prefer the Python-based interfaces.

Conceptual problems with respect to software have been solved, and most functionality has been implemented. No major restructuring has been needed in the last 1.5 years. Software changes necessary for updated or upgraded hardware can be integrated without changing the structure of the software. However, improvements with respect to horizontal scalability of the mapping layer and the ESS are needed for larger systems (NMPM2).

6.4 Integration and Operations: The Next 6 Months

6.4.1 T9.5.2

Wafer: We expect post-processing of the last lot to finish in Month 15.

FCP: All remaining FPGA node boards and Wafer IO boards will be manufactured and tested.

6.4.2 T9.5.3

Depending on the MainPCB production output, SU will receive post-processed wafers, MainPCBs, mechanics and peripheral boards from UHEI and assemble and test all wafer modules, lot-wise.

6.4.3 T9.5.4

Providing improved access for external users will be the main focus. A hardware resource management system, SLURM[14], has been tested. Basic functionality and tests are described in the PhD thesis of Eric Müller[15]. After finalising the evaluation it will become the main user interface for running experiments on the NMPM-1. The next steps will be to link the NM platform interface (cf. T9.3.1) with the local system. Later modifications will focus on shared storage/data access across different backends of the Unified Portal.

[14] http://slurm.schedmd.com/)
[15] https://www.kip.uni-heidelberg.de/Veroeffentlichungen/details.php?id=3112

7. Neuromorphic Computing Platform: User Support and Community Building (WP9.6)

7.1 User Support and Community Building: Overall Goals

The goal of WP9.6 is to assist users, e.g. by teaching them how to use the emerging neuromorphic computing Platforms. The WP's only Task is:

- T9.6.1 Neuromorphic Computing service centre for user training and user support: documentation.

7.2 User Support and Community Building: Main Achievements

A highly detailed specification document—an essential first step for establishing user support—was written during the reporting period (Deliverable D9.7.1). It contains descriptions of both of the hardware systems, software tools, and several use cases. This document is the basis for future users to get involved with the HBP Neuromorphic Computing Systems. We plan to maintain this as a "living document" with continuous updates.

Both systems (MC and PM) have initiated user-training events. For the NM-MC1 system, one user-training workshop with 22 participants took place in April 2014. The NM-PM-1 systems offered a training session at the first HBP School in Alpbach (Austria) in September 2014.

7.3 User Support and Community Building: Main Problems

No problems have been encountered during the first 12 months. The main user training activity will commence when the large systems become available.

7.4 User Support and Community Building: The Next 6 Months

The Subproject will continue to update the specification document[16], and will also offer user training. Specifically, an "HBP Future Computing School" is planned for 2015, which will emphasise training future users of the HBP Neuromorphic Computing Systems.

[16] See footnote 1 on page 7 for access details.

8. Scientific Coordination (WP9.7)

8.1 Scientific Coordination: Internal Meetings

Please see Annex D: Internal Meetings.

8.2 Scientific Coordination: HBP Meetings

Please see Annex E: HBP Meetings.

8.3 Scientific Coordination: External Meetings

Please see Annex F: External Meetings.

8.4 Scientific Coordination: Monitoring & Quality Control

- SP9 is coordinated via monthly videoconferences and quarterly in-person meetings (together with the SP11.3 Partners)
- WP leaders coordinate the different WPs. Several of the WPs are (intentionally) one- or few-partner WPs, thus allowing easy "local" coordination via onsite meetings.
- The HBP Science and Technology Office (STO) collects SKPI values to help the SP leaders to follow plan details.

Annex A: Milestones

No.	Milestone Name	WP	Month Due	Achieved
M173	NM-PM-1 ready for serial production.	9.1	6	Yes
M177	NM-MC-1 ready for serial production.	9.2	6	Yes
M181	Software tools for neuromorphic computing fully specified.	9.3	6	Yes
M183	Detailed specification of research activities on novel neuromorphic technologies.	9.4	6	Yes
M185	Neuromorphic Computing Platform fully specified.	9.5	6	Yes
M188	Requirements for user documentation and support for the Neuromorphic Computing Platform; guidelines for establishing alliances.	9.6	6	Yes
M182	Software tools for NM-PM and NM-MC demonstrated.	9.3	12	Yes
M189	Identification of potential alliances on neuromorphic computing.	9.6	12	Yes

8.5 Additional information regarding MS182 and MS189

8.5.1 M182 Software tools demonstrated

NM-MC1 Software summary

We have completed an initial version of the SpiNNaker toolchain, which allows users to run PyNN scripts on SpiNNaker with a commonly used subset of the full PyNN 0.7 functionality. We are doing a refactor of this software to produce a fully tested and functional implementation, which will cover even more of the PyNN functionality, and will be more reliable going forward. We have an initial version of middleware, which will allow the execution of PyNN scripts on SpiNNaker.

NM-PM1 Software summary

The NM-PM1 user interface supports the PyNN API version 0.7. Initial support for 0.8 has been implemented for the executable system specification (ESS). A scalable mapping layer converts neuronal network descriptions into hardware configurations. The experiment can be executed on the neuromorphic hardware system or, alternatively, on the ESS. The output of all layers can be serialised; this operation mode will be used to dispatch computationally expensive operations to an external compute cluster. An initial version of the resource scheduling system (based on SLURM) has been deployed. Jobs submitted to the NMPI portal are executed on a prototype wafer that is managed by SLURM. Results data are provided using the WEBDAV protocol.

8.5.2 M189 Alliance identified

International Alliances in Neuromorphic Computing

Neuromorphic Computing (NMC) is a radically new approach to information processing that is based on the principles of computing in neural circuits. The potential advantages in terms of energy efficiency, the ability to learn, and robustness can only be exploited and transferred to applications if custom hardware systems are constructed and operated. SP9 is working along these lines with two unique systems (NM-MC-1 and NM.PM-1) currently under construction. During the first Project year, international contacts have led to two major alliances with the US and China:

1) The EU-US Alliance in Neuromorphic Computing. Together with US Partners, SP9 has established an excellent scientific alliance, which has led to a series of well-attended workshops. The goal of this new workshop series is to share recent developments, and to work towards a worldwide strategy for neuromorphic computing. The series started with an initial workshop in Heidelberg (Germany) and

continued with a series of workshops in Albuquerque (New Mexico). The workshop is jointly organised by EU and US groups, with Karlheinz Meier (Heidelberg) as the European representative on the scientific organising committee. So far, three very successful workshops have been held, and the next is already planned for 2015.

- The Joint EU-US Workshop on Cortical Processors, Heidelberg, October 15 and 16, 2013
- The Neuro-Inspired Computational Elements (NICE) Workshop Series Information Processing and Computation Systems beyond von Neumann/Turing Architecture and Moore's Law Limits Held in Albuquerque (New Mexico, USA):
  - Local organisation by Sandia Labs 1st Workshop: February 25, 26, and 27, 2013
  - 2nd Workshop: February 24, 25, and 26, 2014
  - 3rd Workshop: (9) February 23, 24 and 25, 2015 (planned).

2) The EU-China Alliance on Neuromorphic Computing. China is preparing a Brain Initiative similar to those in Europe and the US. As in Europe, neuromorphic computing is expected to play a major role in the Chinese initiative. The Chinese key players in the field have therefore initiated a workshop series to align their planning with the work carried out on the international scale, with special emphasis on Europe. So far, two international workshops have been organised in China for this purpose. The HBP was represented at both workshops.

- Symposium on Neuromorphic Systems and Cyborg Intelligence 1st Symposium: July 11 2014, Beijing (China)
- 2nd Symposium: October 19 2014 in Hangzhou, China.

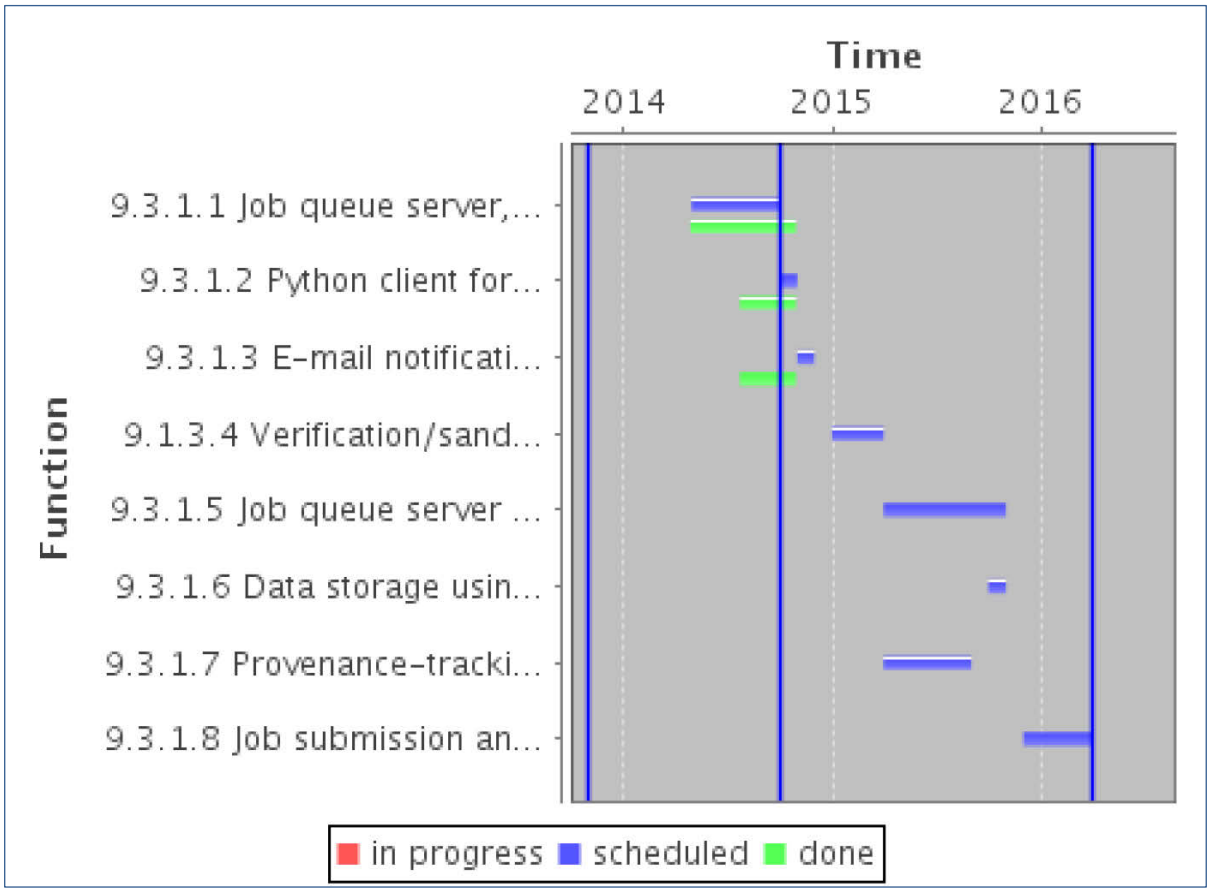
Annex B: Subproject Functions

8.6 T9.3.1 NCS integration with the Brain Simulation and High Performance Computing platforms

NCS integration with the Brain Simulation and High Performance Computing platforms

- 9.3.1.1 Job queue server, minimal. Planned: 2014/04/30 - 2014/09/30
- 9.3.1.2 Python client for job queue REST API. Planned: 2014/09/30 - 2014/10/31
- 9.3.1.3 E-mail notifications. Planned: 2014/10/31 - 2014/11/30
- 9.1.3.4 Verification/sandboxing. Planned: 2014/12/31 - 2015/03/31
- 9.3.1.5 Job queue server with central authentication. Planned: 2015/03/31 - 2015/10/31
- 9.3.1.6 Data storage using resources provided by Neuroinformatics or HPC Platforms. Planned: 2015/09/30 - 2015/10/31
- 9.3.1.7 Provenance-tracking of Neuromorphic jobs. Planned: 2015/03/31 - 2015/08/31
- 9.3.1.8 Job submission and retrieval using Brain Simulation Platform. Planned: 2015/11/30 - 2016/03/31

Responsible: andrew.davison@unic.cnrs-gif.fr



Marked in the graphics are Months 1,12 and 30.

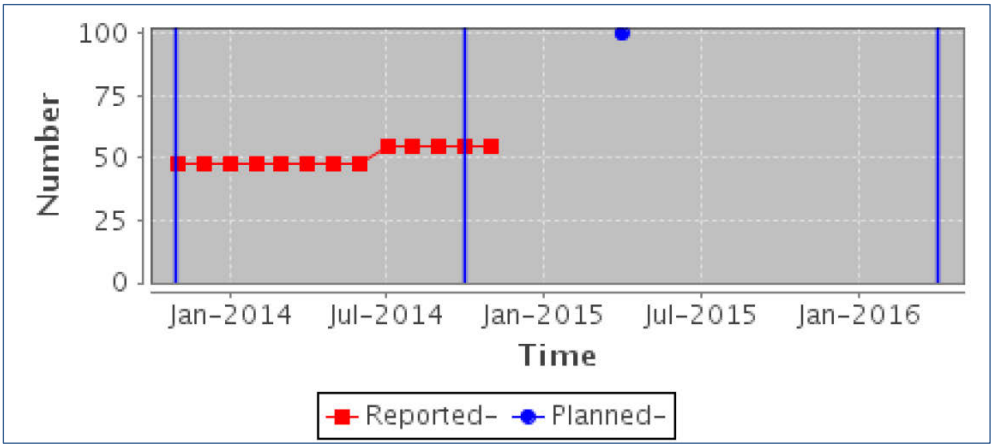
Annex C: Numeric Scientific Key Performance Indicators (SKPIs)

The graphs show the development of defined numerical SKPI values, which help the SP to track its own progress, and which serve as early warning indicators for the STO (Science and Technology Office). An up-to-date view of the KPI information is always accessible to project members online. The graphics here are an export from the online tool. Marked in the graphics are Months 1,12 and 30. The graphs were exported during the finalisation of the Deliverable text (end of November 2014) and therefore, some of the graphs show values after the end of Month 12 (second blue line).

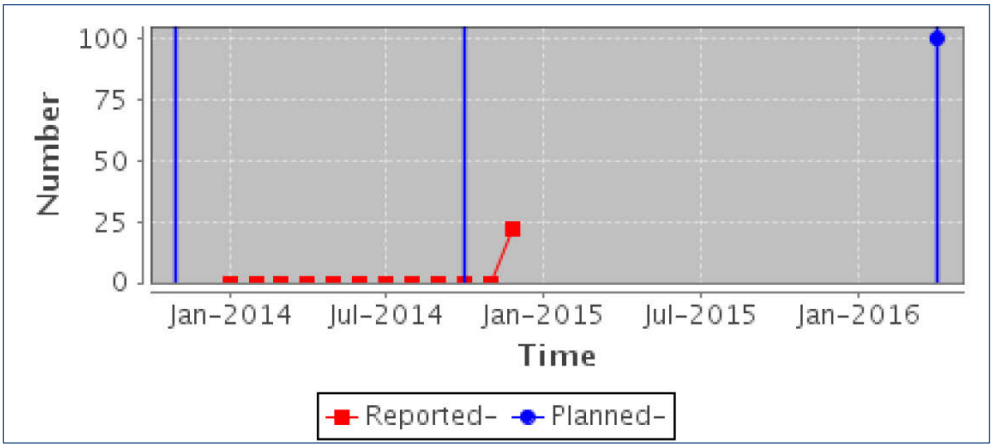
8.7 Neuromorphic computing with physical emulation of brain models

8.7.1 T9.1.5 Development of low level software and firmware for the neuromorphic system

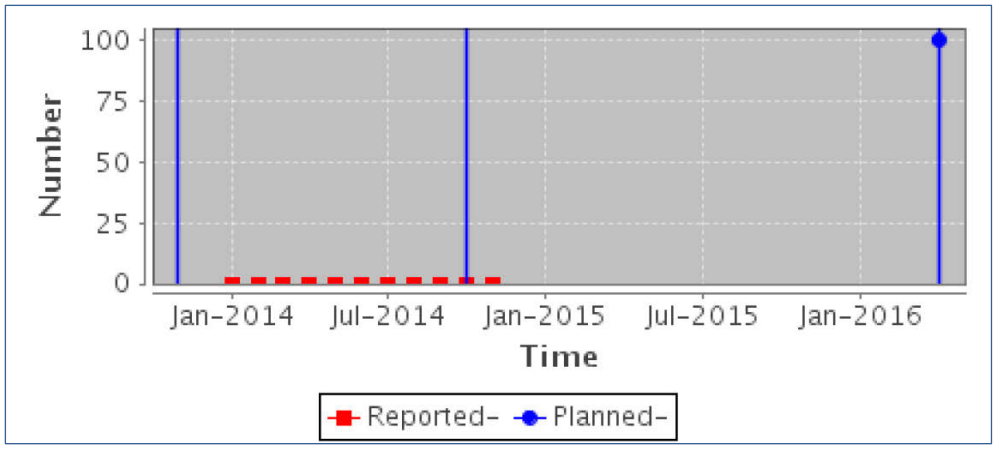
- Code coverage of hardware abstraction layers. Responsible: mueller@kip.uni-heidelberg.de



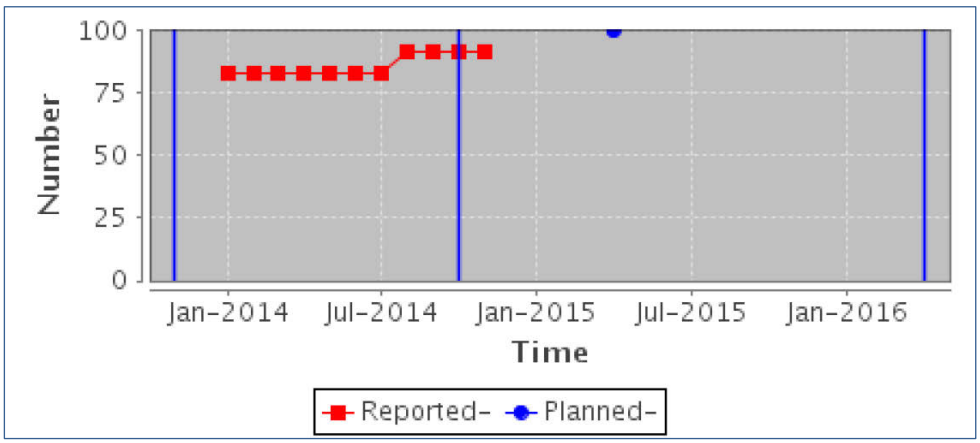
- Code coverage of calibration toolchain. Responsible: mueller@kip.uni-heidelberg.de



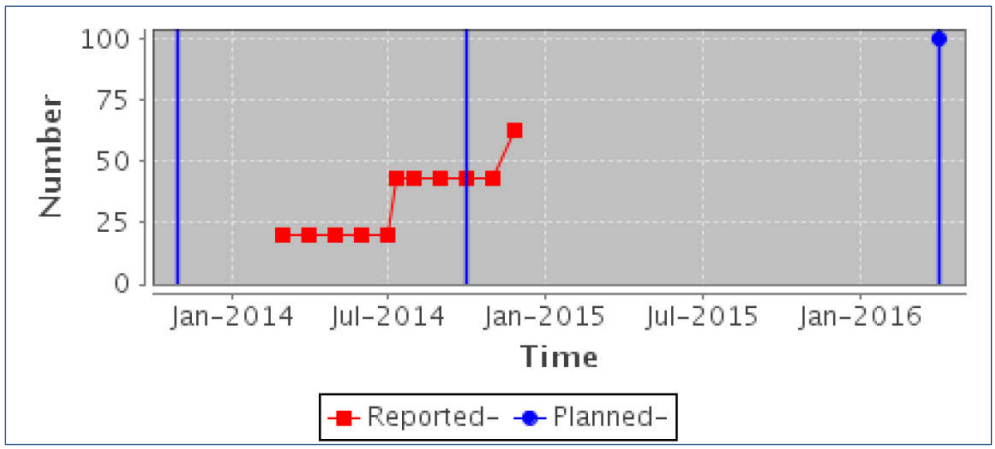
- Code coverage of frontend and mapping layer. Responsible: mueller@kip.uni-heidelberg.de



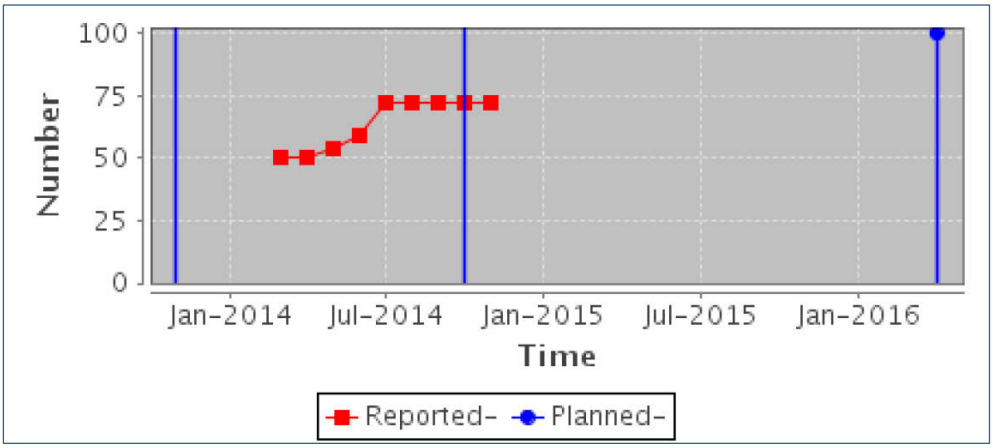
- Func. coverage of hardware abstraction layers. Responsible: mueller@kip.uni-heidelberg.de.



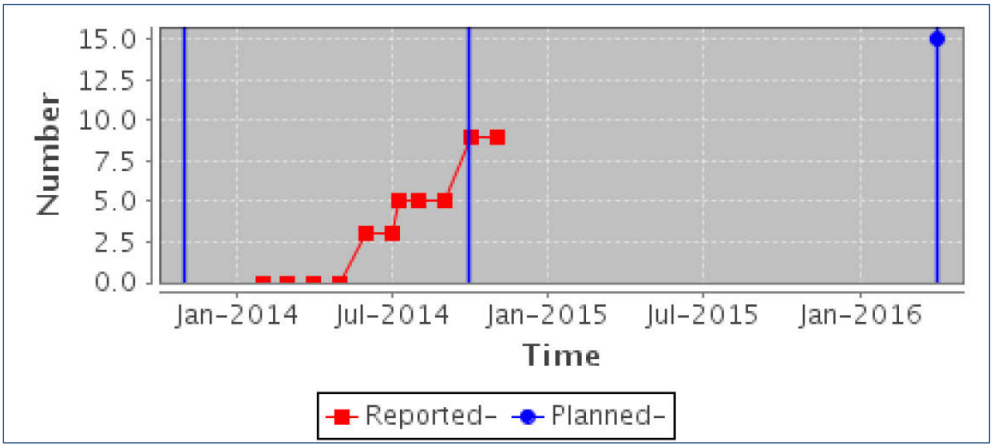
- Func. coverage of calibration toolchain. Responsible: mueller@kip.uni-heidelberg.de



- Func. coverage of frontend and mapping layer. Responsible: mueller@kip.uni-heidelberg.de.

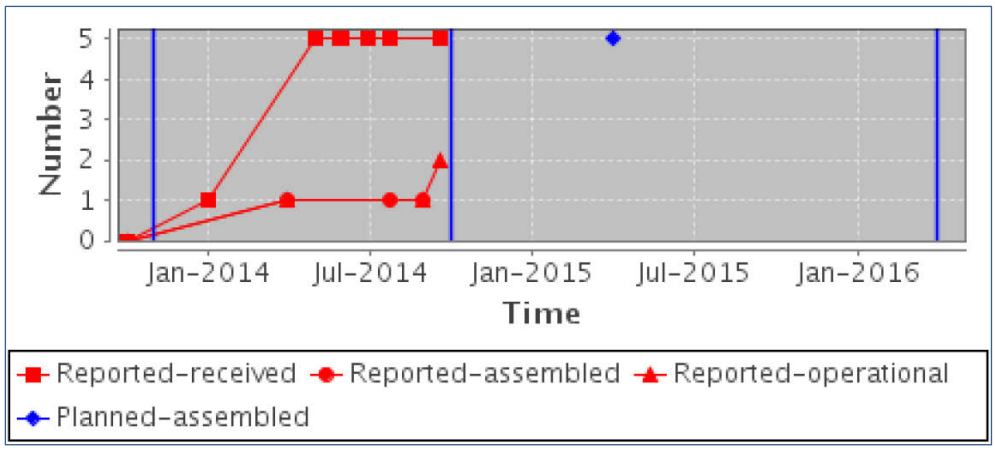


- Number of calibration routines for hardware model parameters. Responsible: mueller@kip.uni-heidelberg.de

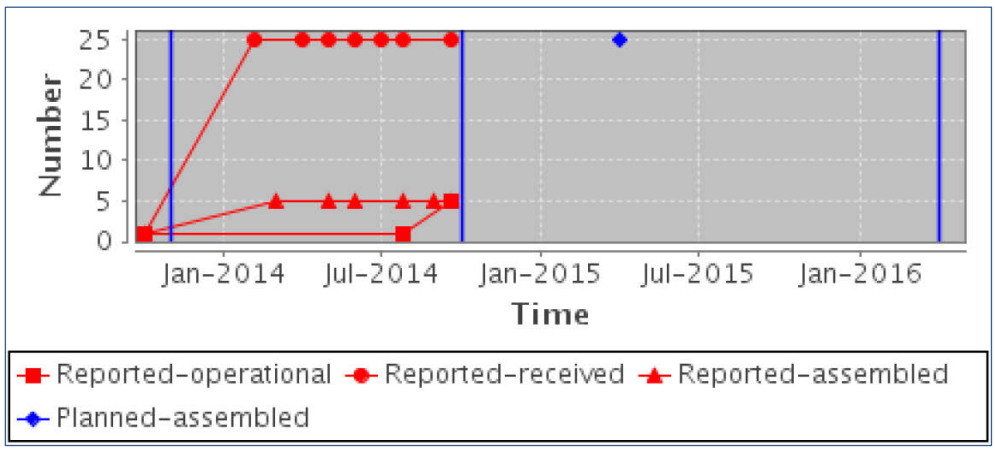


8.8 WP9.2 Neuromorphic computing with digital many-core implementation of brain models

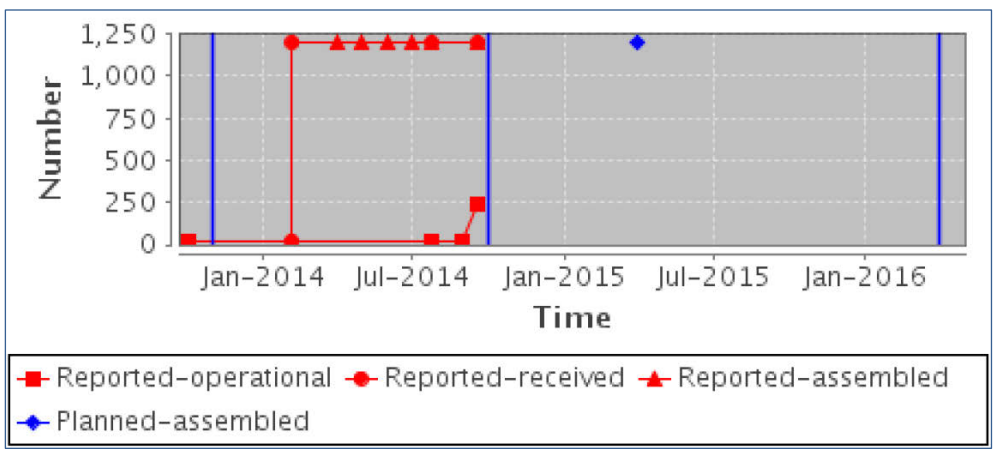
- NMMC Cabinet Assembly Cabinet (47U). Responsible: david.r.lester@manchester.ac.uk



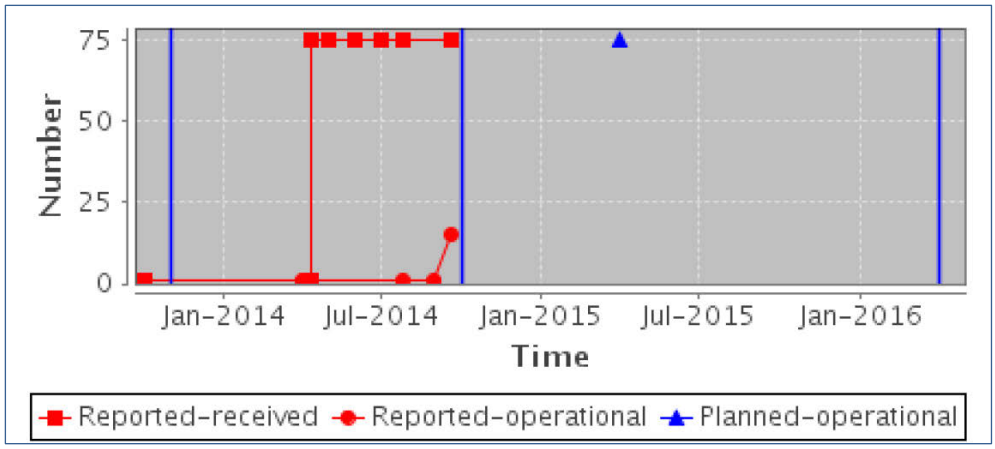
- NMMC Sub-rack assembly_1 6U sub-rack. Responsible: david.r.lester@manchester.ac.uk



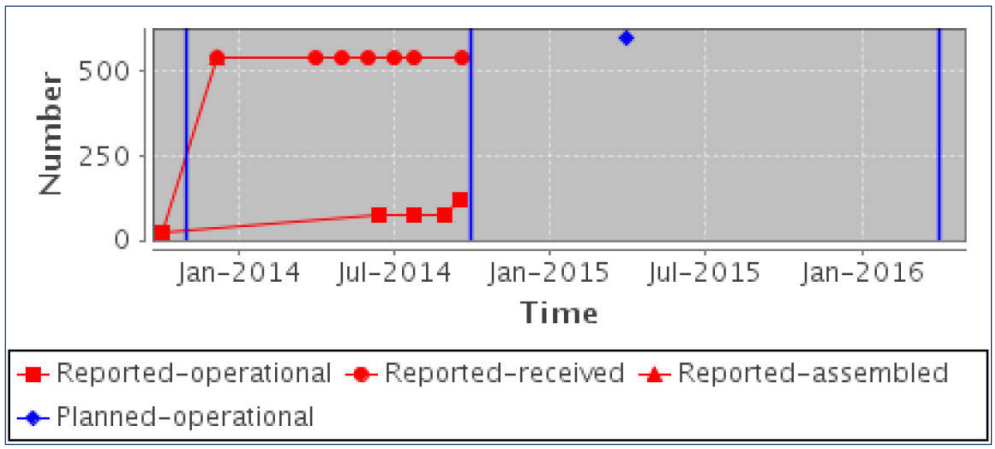
- NMMC Sub-rack assembly_2 Card guides. Responsible: david.r.lester@manchester.ac.uk



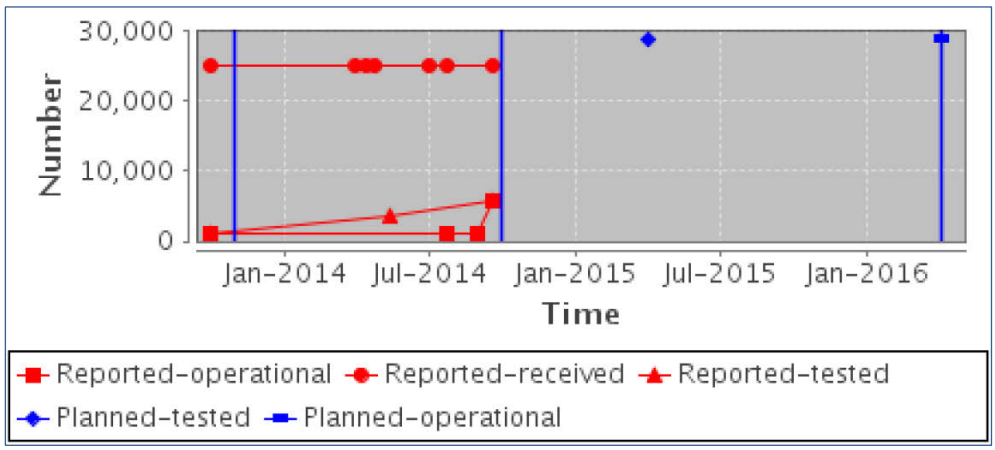
- NMMC Sub-rack assembly_3 Backplane PCB. Responsible: david.r.lester@manchester.ac.uk



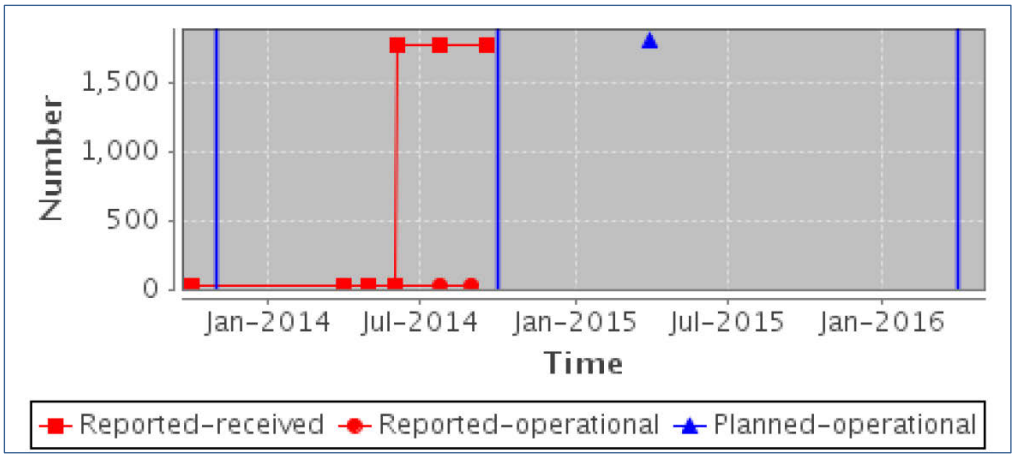
- NMMC Sub-rack assembly_4 Spin5 PCB. Responsible: david.r.lester@manchester.ac.uk



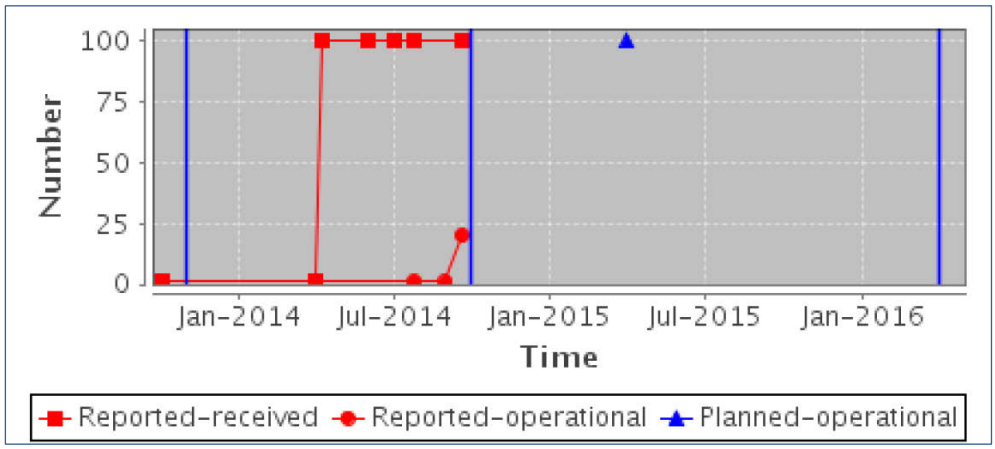
- NMMC Sub-rack assembly_5 SpiNNaker chip. Responsible: david.r.lester@manchester.ac.uk



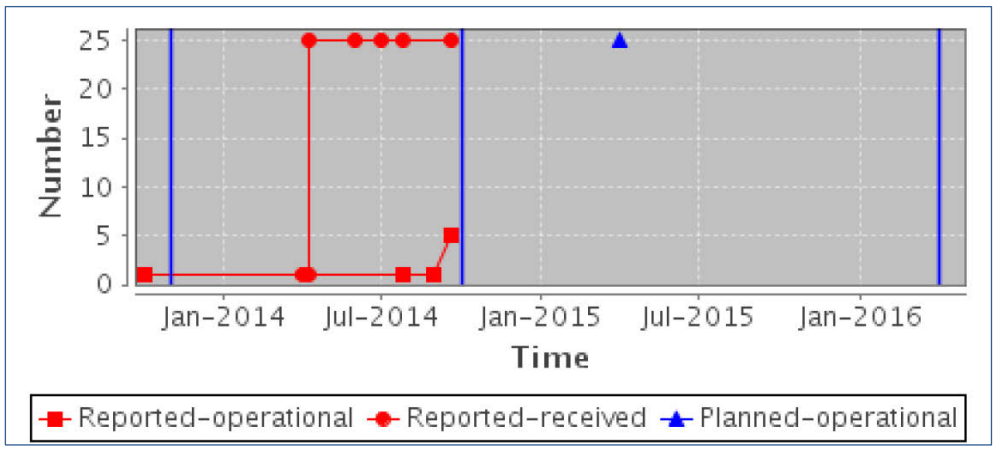
- NMMC Sub-rack assembly_6 SATA cables. Responsible: david.r.lester@manchester.ac.uk



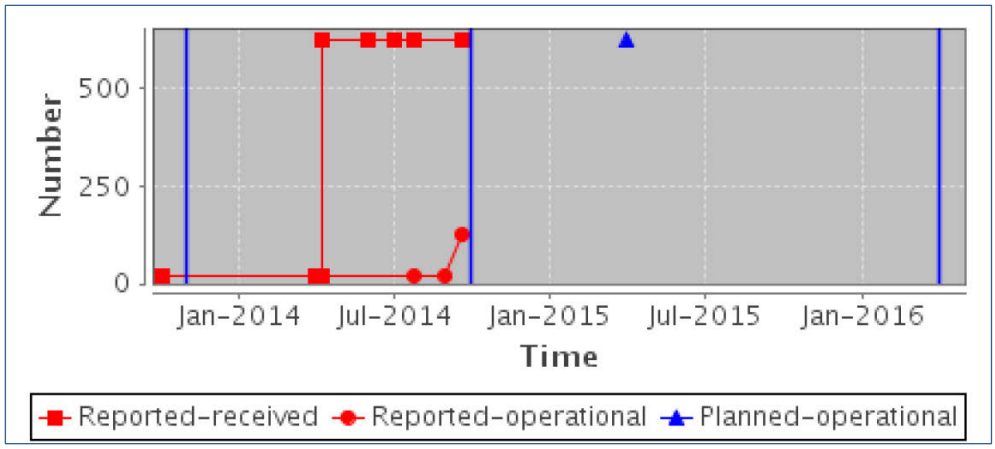
- NMMC Sub-rack assembly_7 Mains cables. Responsible: david.r.lester@manchester.ac.uk



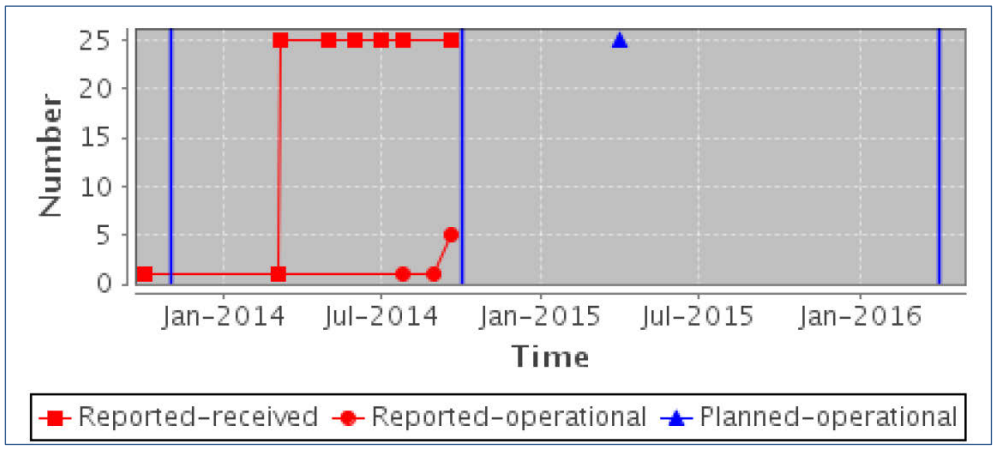
- NMMC Network_1 Switch Netgear FS726T. Responsible: david.r.lester@manchester.ac.uk



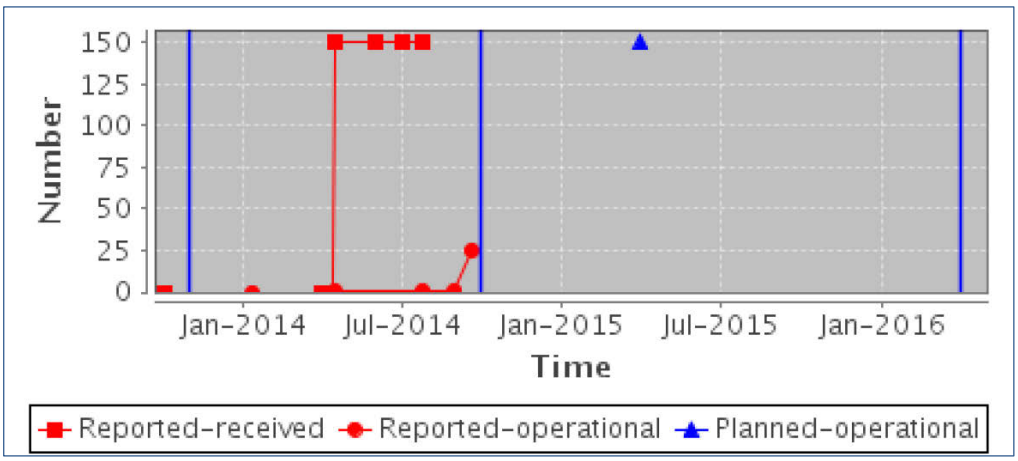
- NMMC Network_2 Network cables. Responsible: david.r.lester@manchester.ac.uk



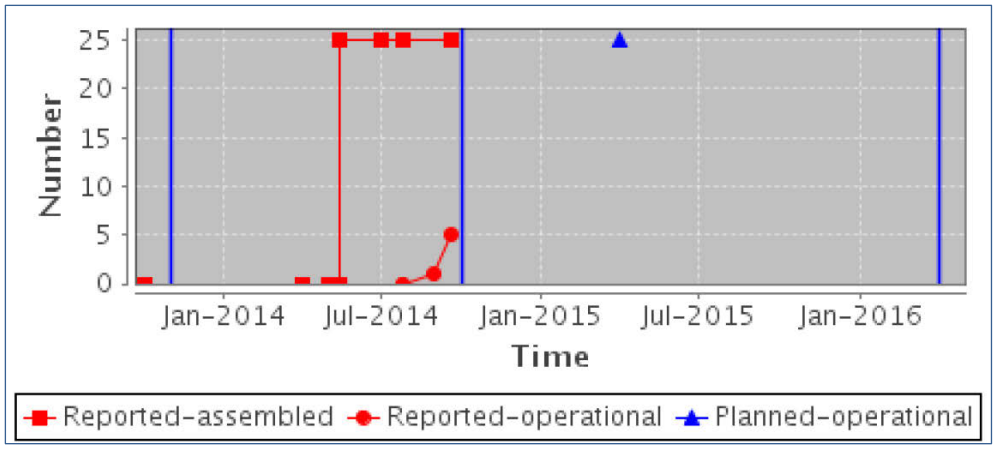
- NMMC Fan Tray Assembly_1 Fan tray metalwork. Responsible: david.r.lester@manchester.ac.uk



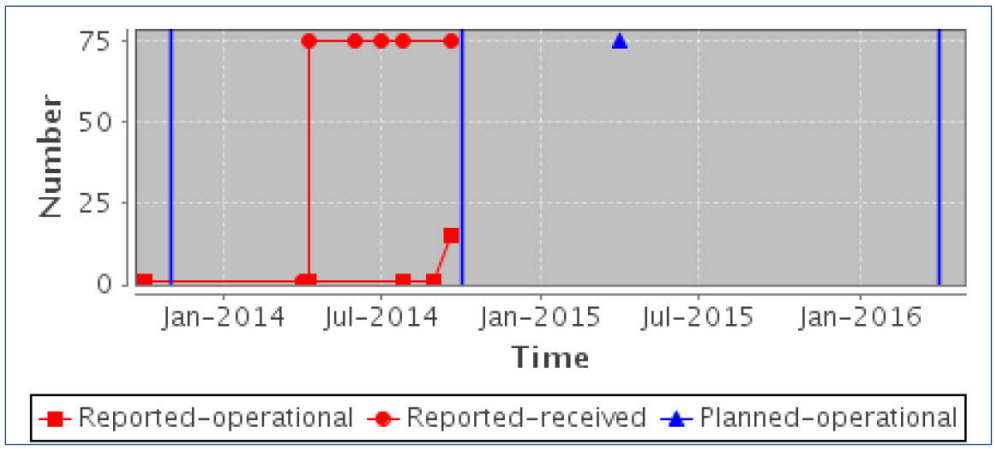
- NMMC Fan Tray Assembly_2 120mm fan. Responsible: david.r.lester@manchester.ac.uk



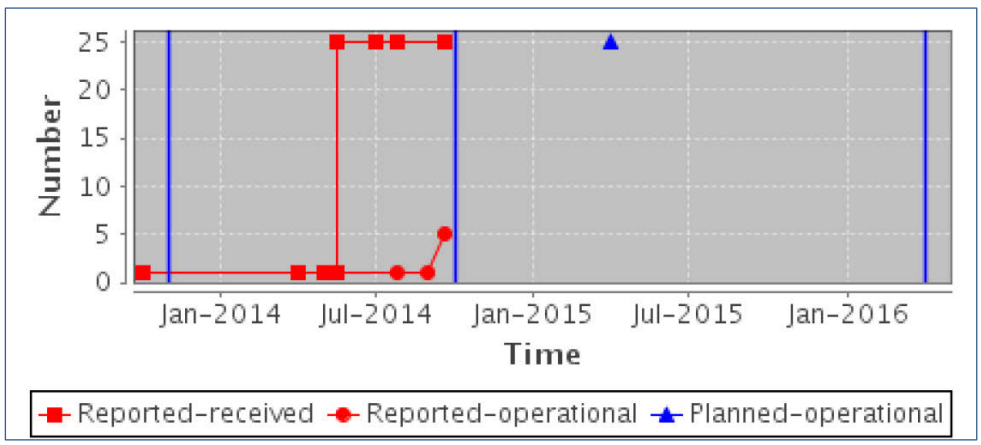
- NMMC Fan Tray Assembly_3 Display module. Responsible: david.r.lester@manchester.ac.uk



- NMMC Power Supply Assembly_1 Power supply unit (650W). Responsible: david.r.lester@manchester.ac.uk



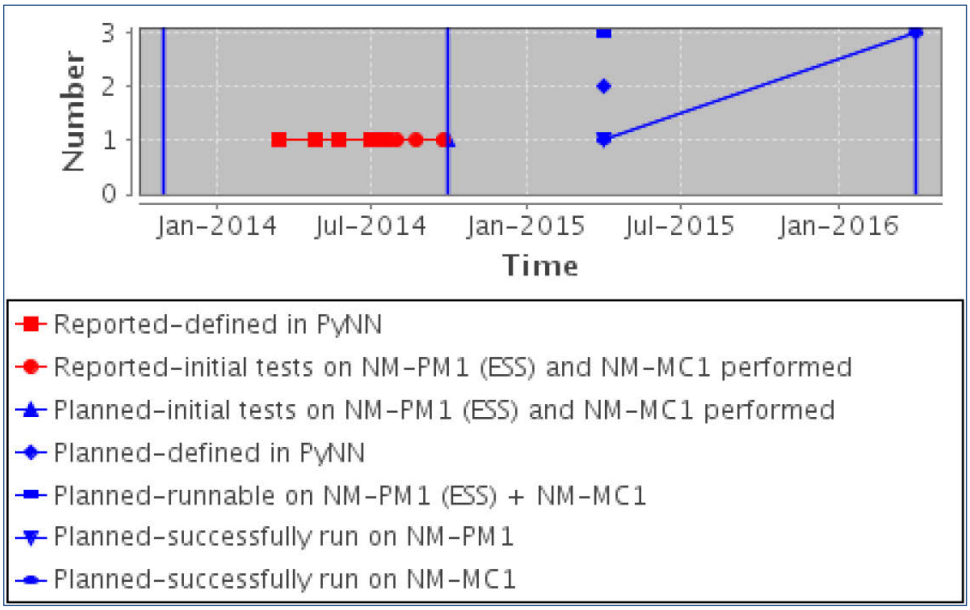
- NMMC Power Supply Assembly_2 Power supply panel. Responsible: david.r.lester@manchester.ac.uk



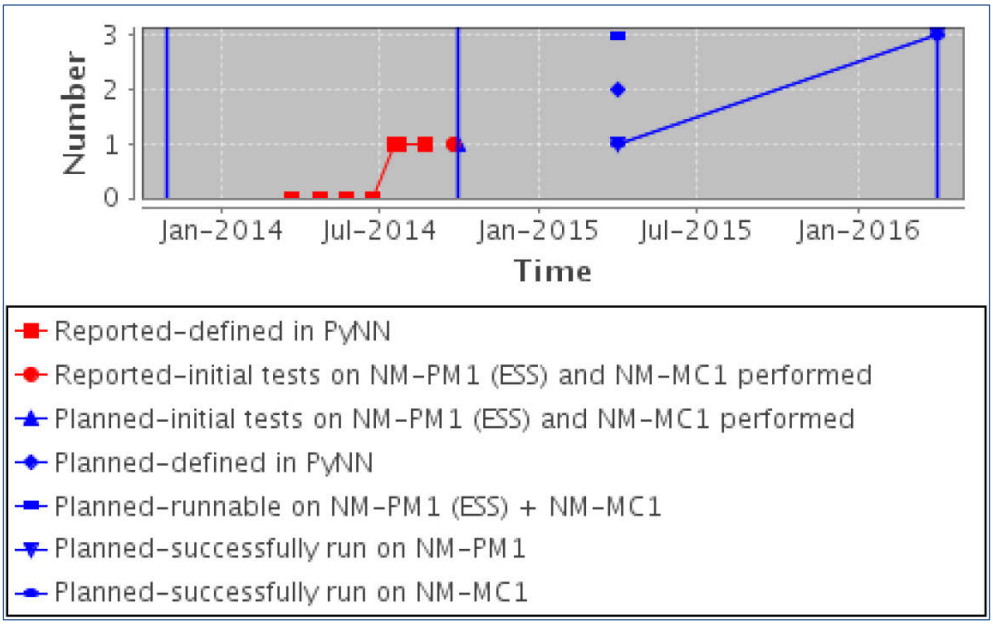
8.9 WP9.3 Software tools for neuromorphic computing

8.9.1 T9.3.4 Benchmarking the neuromorphic circuits developed in WP9.1 and WP9.2

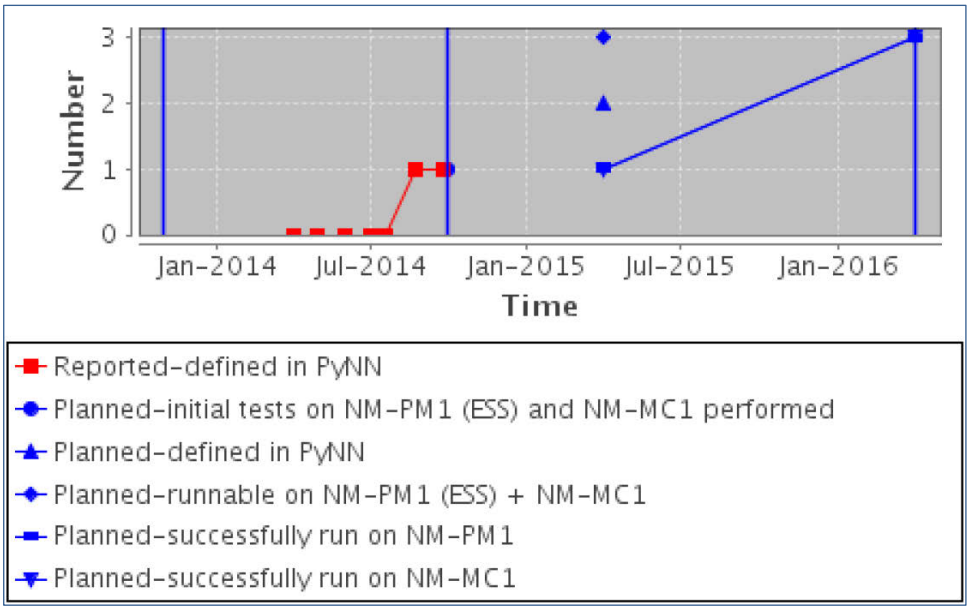
- Benchmark for Neuron. Responsible: ala@csc.kth.se



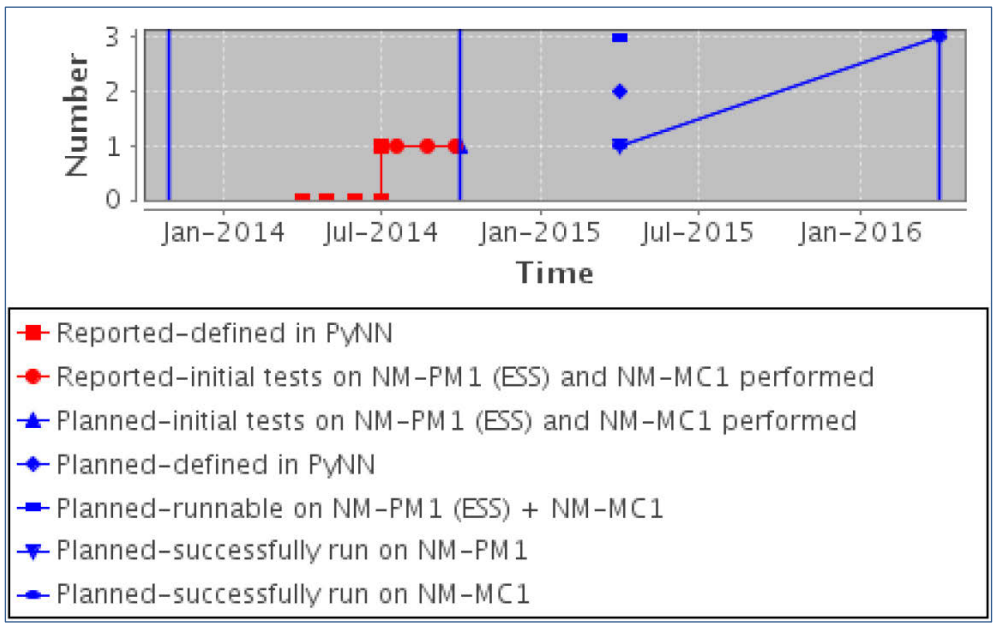
- **Benchmark for Synapses**. Responsible: ala@csc.kth.se



- Benchmark for Microcircuits. Responsible: ala@csc.kth.se

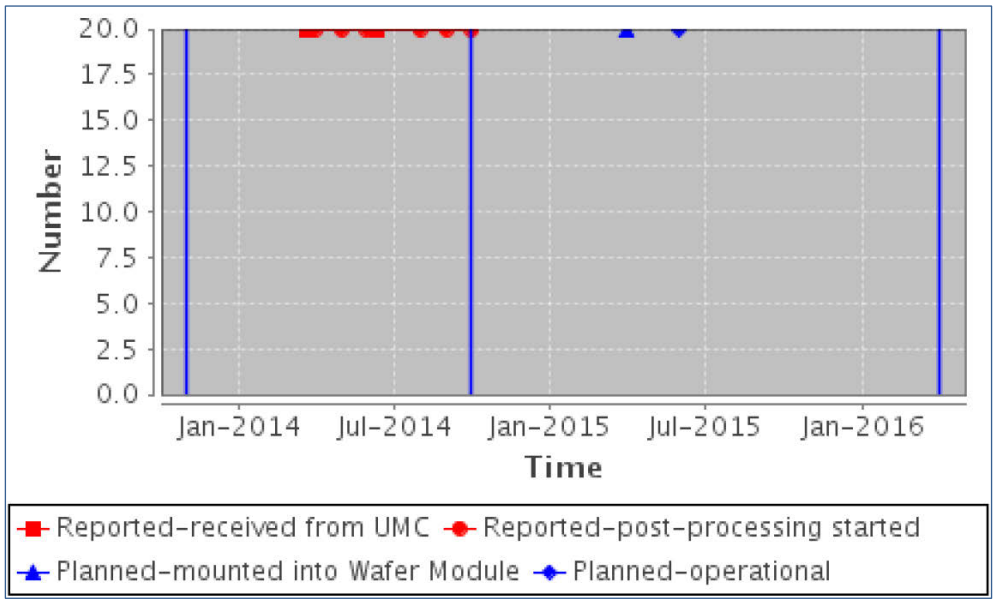


- Benchmark for Networks. Responsible: ala@csc.kth.se.

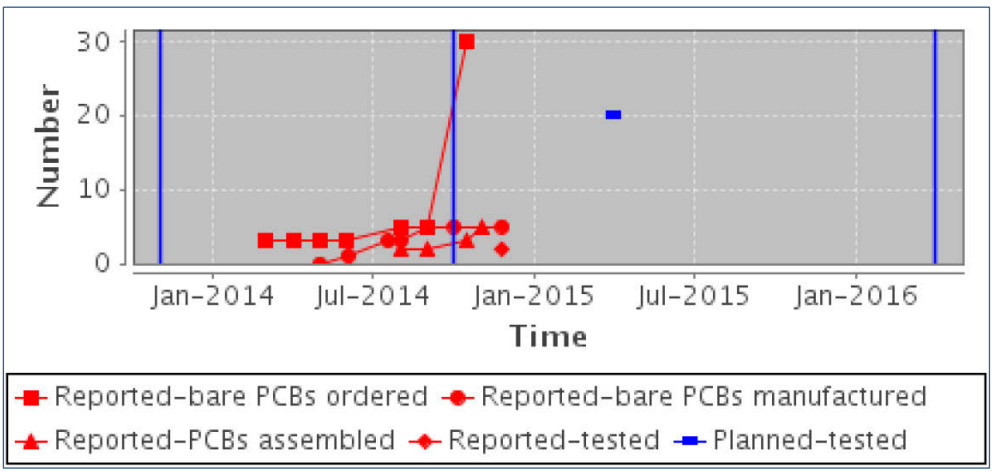


8.10 WP9.5 Neuromorphic Computing Platform: integration and operations

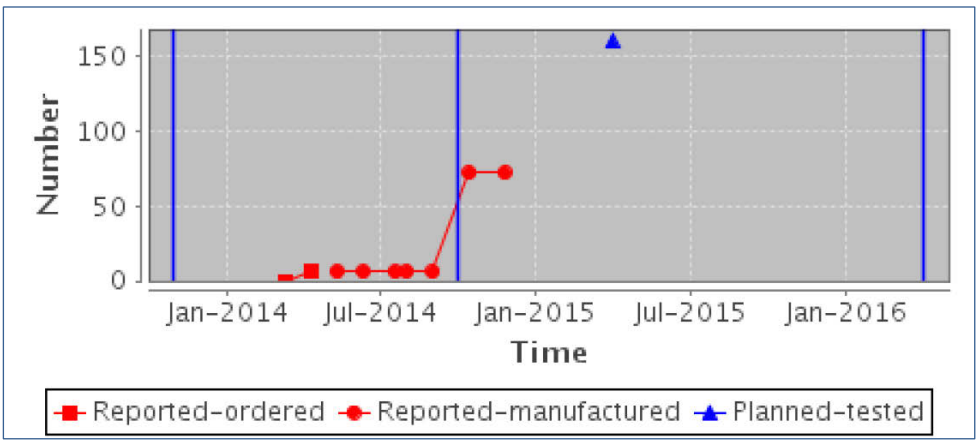
- Wafer. Responsible: agruebl@kip.uni-heidelberg.de



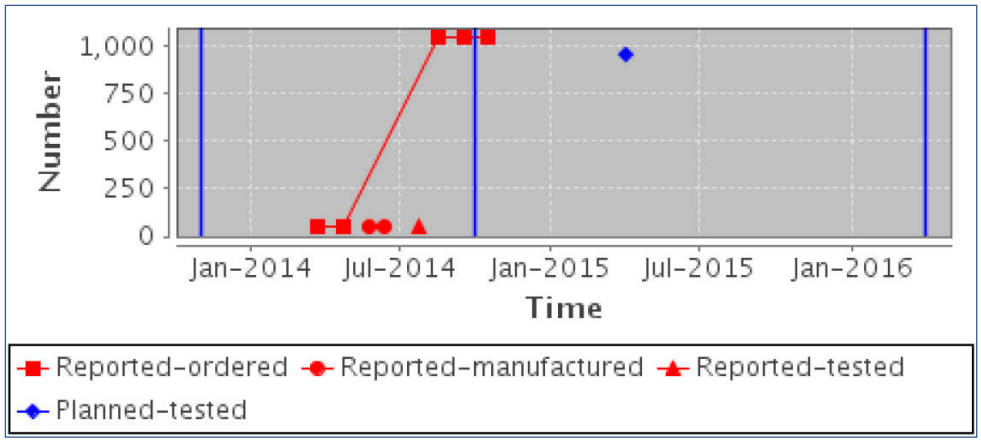
- MainPCBs. Responsible: husmann@kip.uni-heidelberg.de



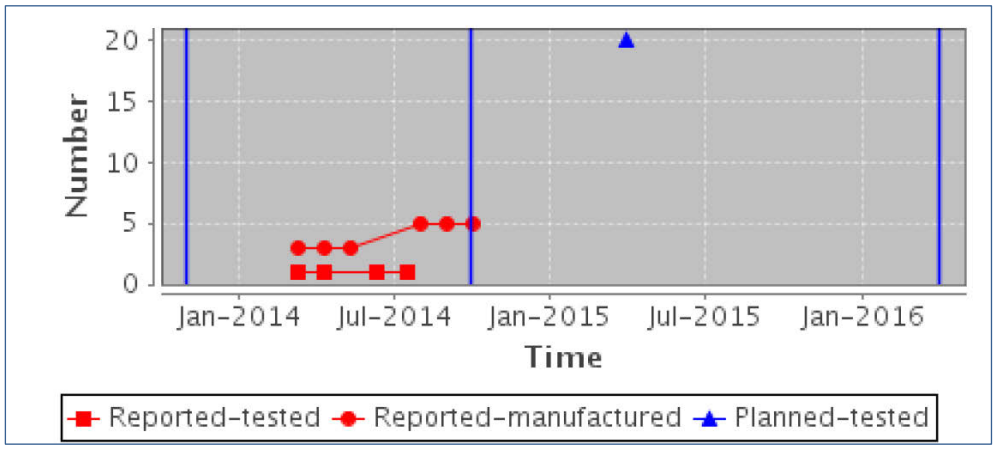
- CURE Monitoring and Control PCB. Responsible: husmann@kip.uni-heidelberg.de



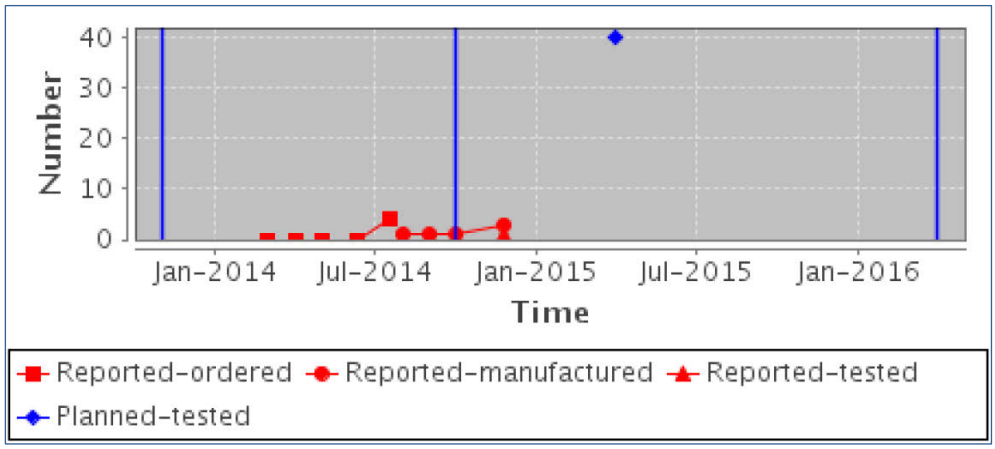
- FCP: FPGA Communication PCB. Responsible: stefan.schiefer@tu-dresden.de



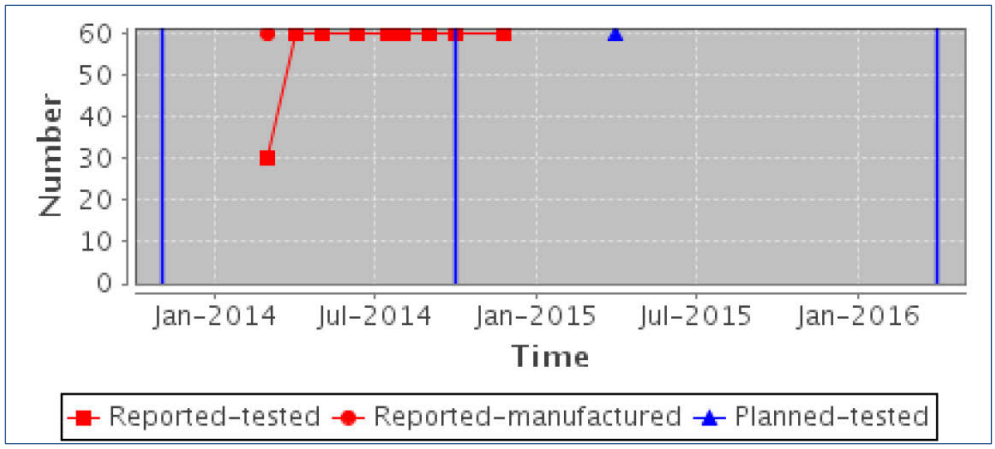
- PowerIt Main Power Supply PCB. Responsible: husmann@kip.uni-heidelberg.de



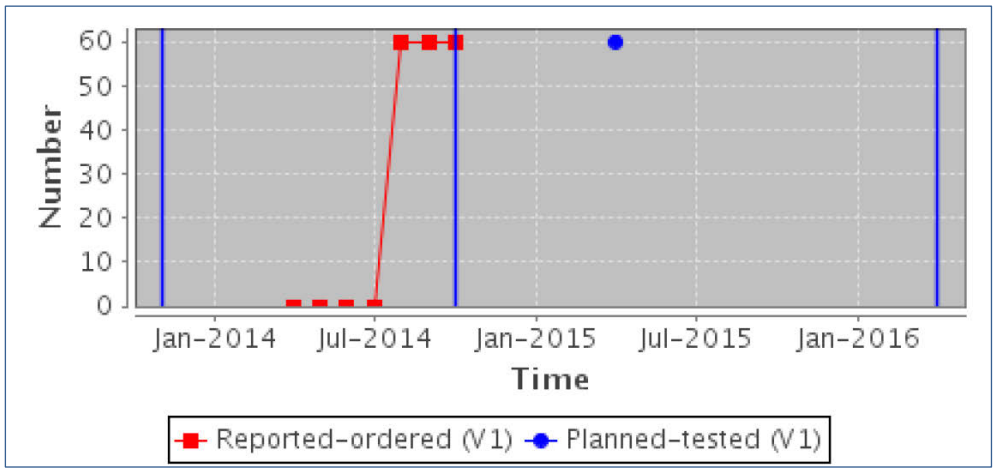
- AuxPwr: Auxiliary Power Supply PCB. Responsible: husmann@kip.uni-heidelberg.de



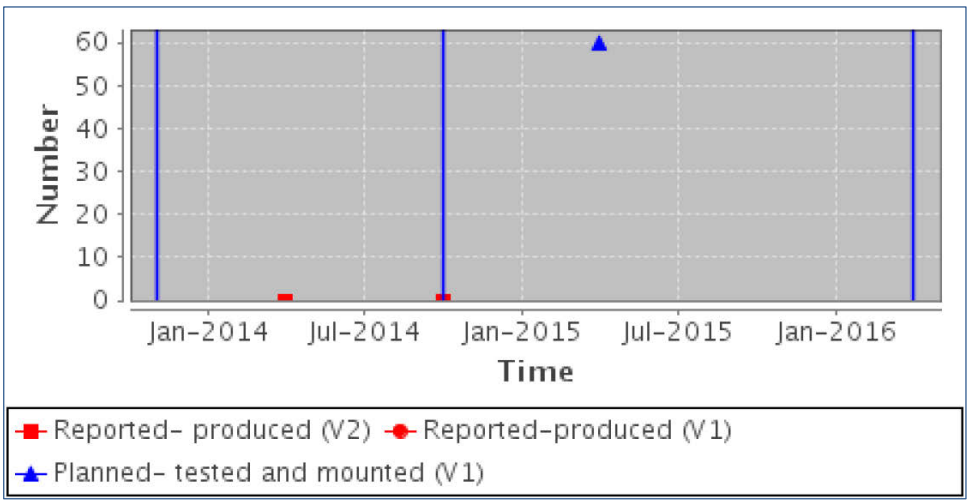
- Analogue Readout Component Flyspi. Responsible: husmann@kip.uni-heidelberg.de



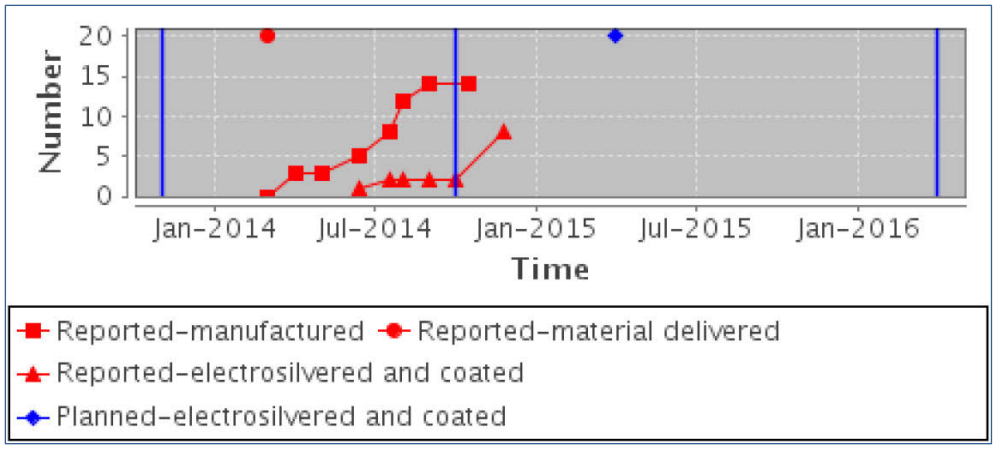
- Analogue Readout Component AnaFP. Responsible: agruebl@kip.uni-heidelberg.de



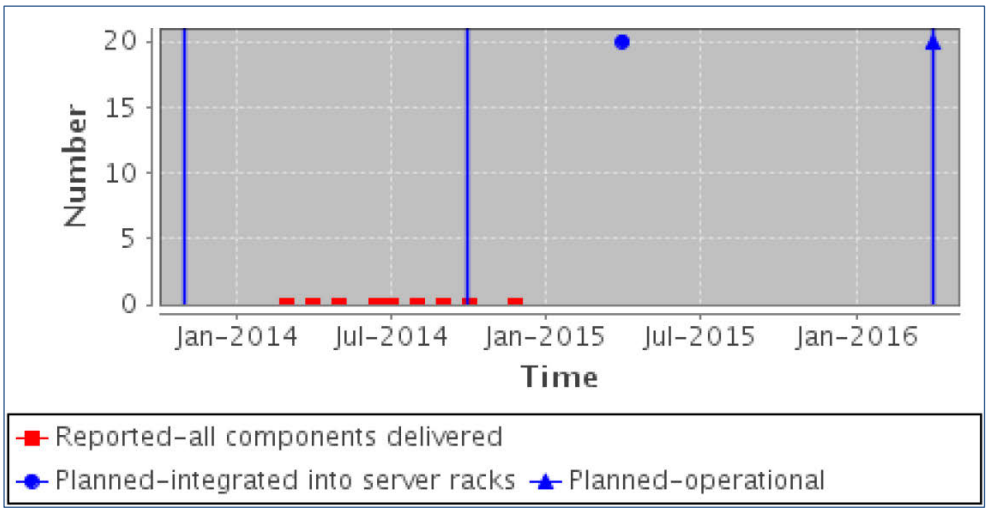
- Analogue Readout Component AnaRM. Responsible: agruebl@kip.uni-heidelberg.de



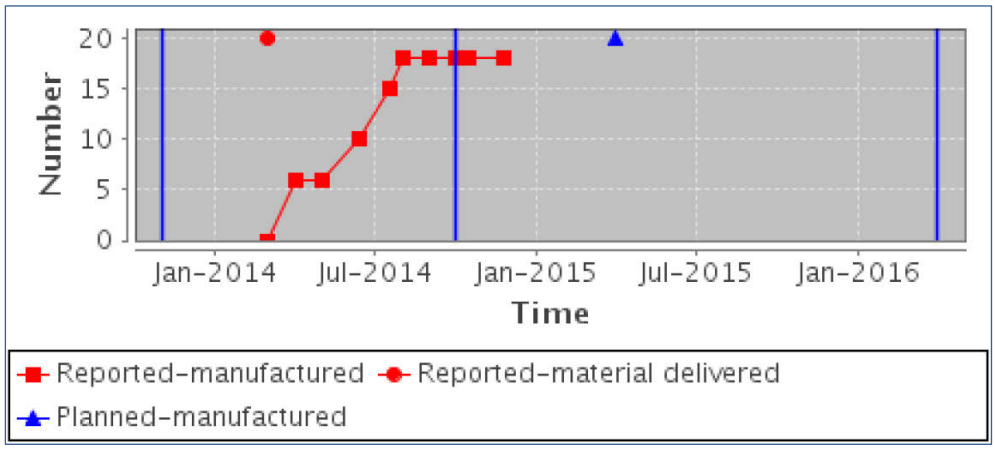
- Mech. component: Top Cover (ToCo). Responsible: husmann@kip.uni-heidelberg.de



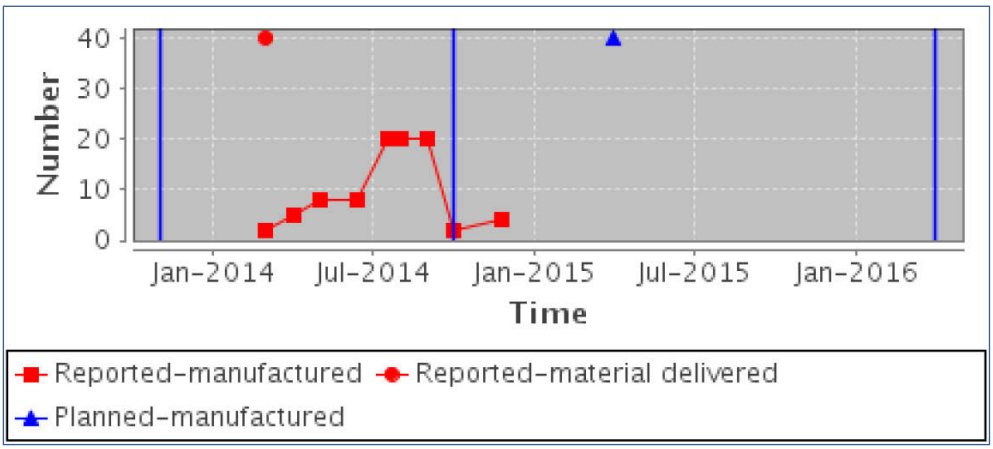
- Wafer Modules. Responsible: husmann@kip.uni-heidelberg.de



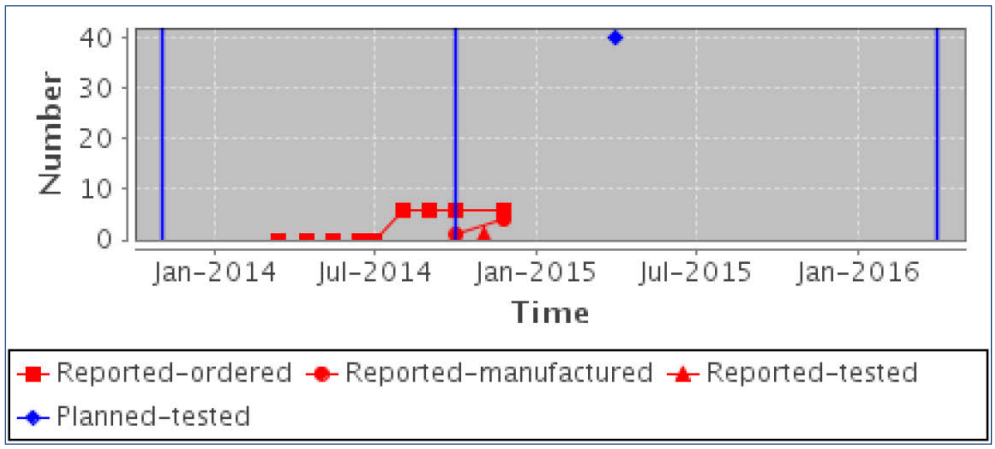
- Mech. component: Wafer Bracket (WBr). Responsible: husmann@kip.uni-heidelberg.de.



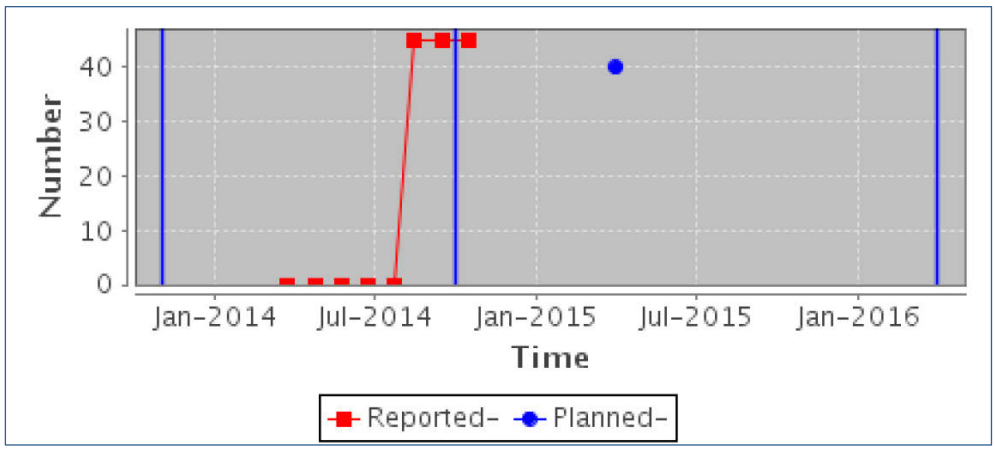
- Mech. component: Positioning Mask for Elastomeric Stripe Connectors (PMk)
  Responsible: husmann@kip.uni-heidelberg.de
- Comment for the re-start in October 2014: due to differences in the new elastomeric delivery (size of the connector stripes) new masks have to be produced. Therefore, the "reported manufactured" number starts again at 0 in October.



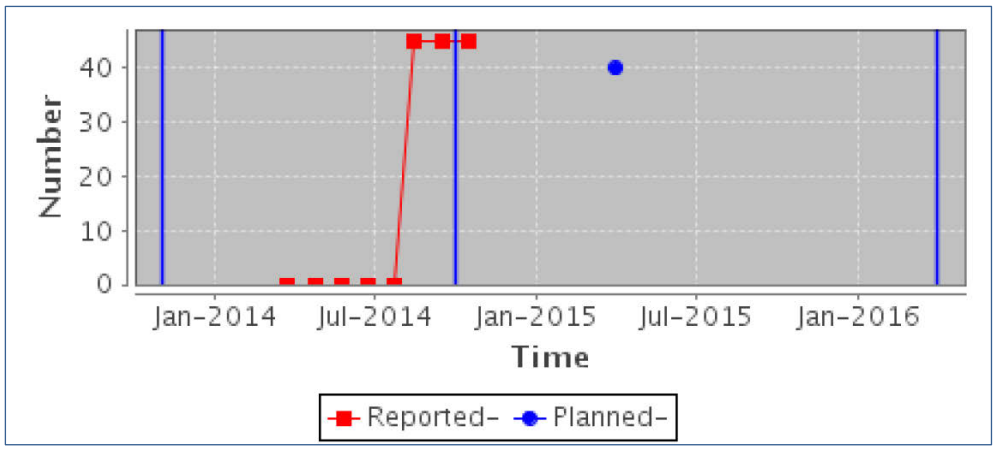
- Breakout boards for the analogue readout signals of the wafer (AnaB). Responsible: husmann@kip.uni-heidelberg.de



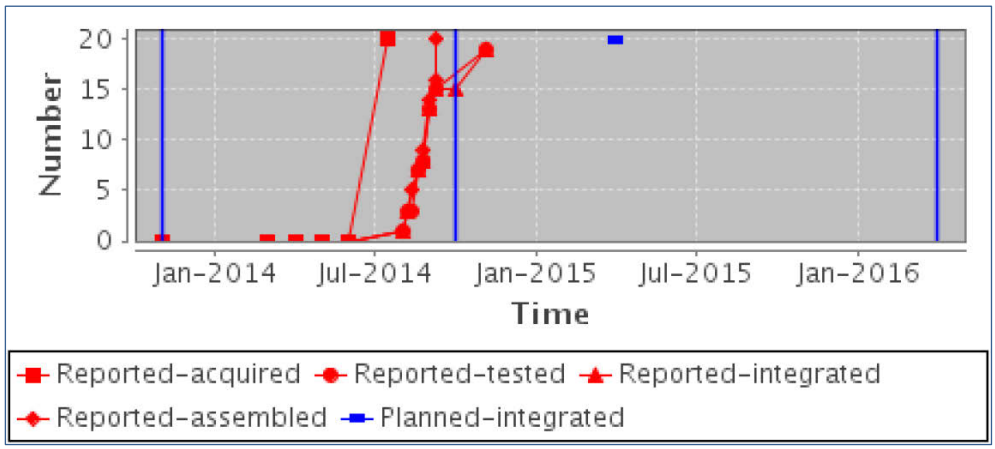
- WIOV: Physical Layer and comm. boards with vertical orientation. Responsible: stefan.schiefer@tu-dresden.de



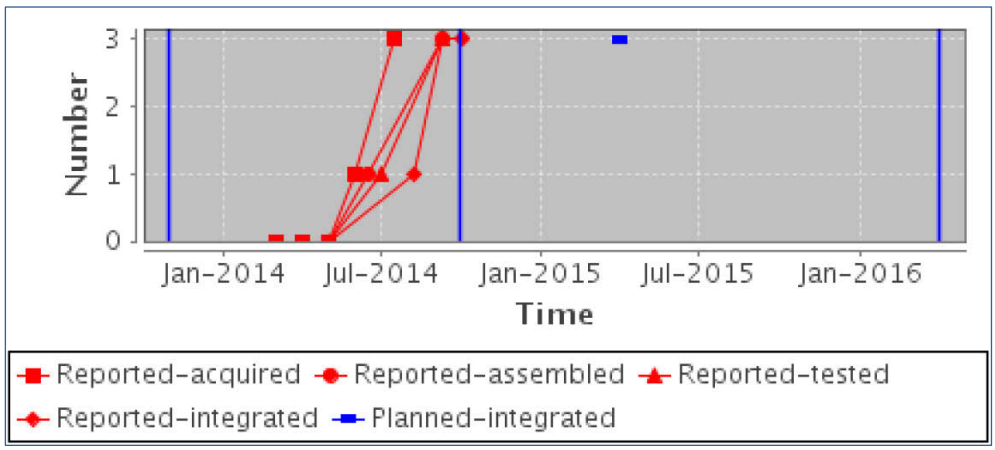
- WIOH: Physical Layer and comm. boards with horizontal orientation. Responsible: stefan.schiefer@tu-dresden.de



- NM-PM Cluster nodes. Responsible: mueller@kip.uni-heidelberg.de

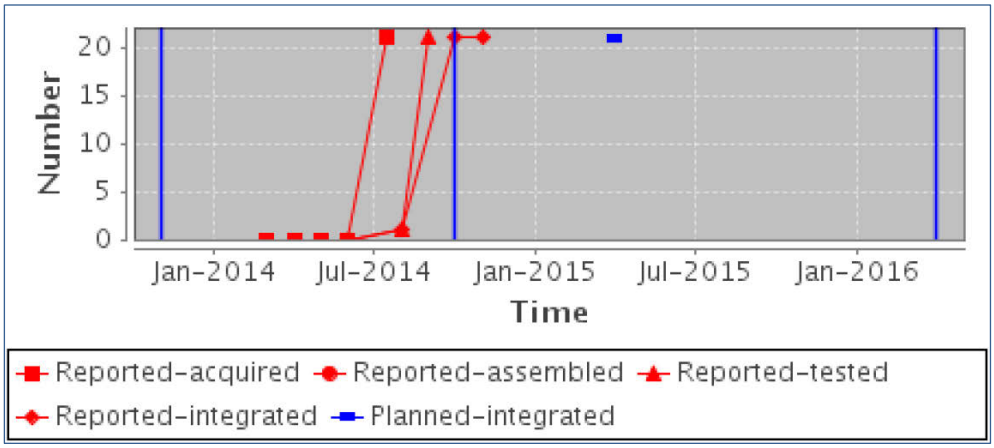


- NM-PM Server nodes. Responsible: mueller@kip.uni-heidelberg.de



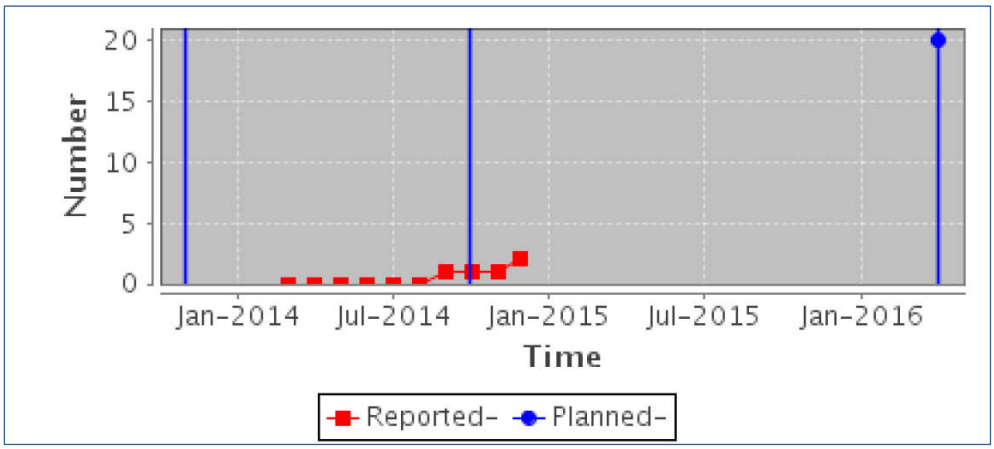
- NM-PM Wafer module and backbone switches. Responsible: mueller@kip.uni-heidelberg.de
  - 2014/08/01 (value 1): top-of-rack switch

- 2014/08/01 (value 1): top-of-rack switch
- 2014/09/01 (value 21): +all wafer switches tested
- 2014/10/01 (value 21): +all wafer switches integrated

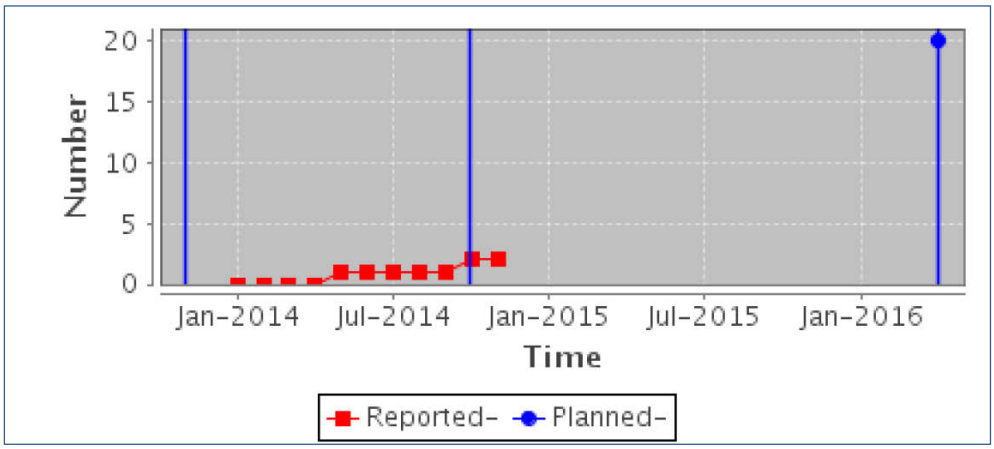


8.10.1 T9.5.3 Neuromorphic Computing Systems - assembly, operation & maintenance

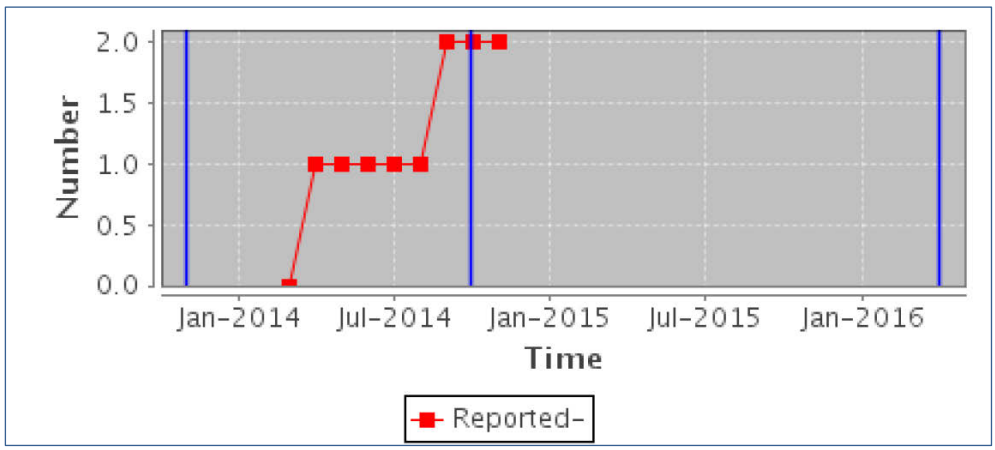
- Number of defect maps available (1/wafer). Responsible: mueller@kip.uni-heidelberg.de



- Wafers available for PyNN users. Responsible: mueller@kip.uni-heidelberg.de
  - 2014/05/01 (value 1): Default software stack available on prototype #0 since ~May… testing started much earlier.
  - 2014/07/01 (value 1): Testing of next wafer system started, but not yet a/v for PyNN users
  - 2014/10/01 (value 2): second prototype available via SLURM



- Number of neural network experiments executed. Responsible: mueller@kip.uni-heidelberg.de
  - 2014/07/01 (value 1): "Hellfire" chain (sjeltsch)
  - 2014/09/01 (value 2): Sebastian Schmitt starts to experiment with Synfire Chain using multiple HICANNs



Annex D: Internal Meetings

Start Date	Subject	Description	Location
2013-10-01 14:00:00.0	SP9 NMPM1 Software Video Conference (UNIC/TUD/UHEI)	Main topics: Halbe FPGA: functions and handling of spikes Syncing Systime counter on multiple HICANNs LiveCD Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20131001	Video conference
2013-10-02 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: J. Partzsch, V. Thanasoulis, (S. Hartmann), S. Schiefer, C. Koke, E. Müller, V. Karasenko, S. Friedmann, A. Grübl Main topics: Coordination of reticle and multi-reticle synchronisation Errors in mixed pulse/config operation Strong Pulse activity from HICANN can block config traffic in experiments, although config is prioritised in HICANN Reliability and current state of DNC-HICANN high-speed connections Control of total experiment runtime Visiblity of FPGA debug features to user SDRAM clock speed on Virtex5 board Repository structure Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20131002	TelCo
2013-10-22 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: Andreas Grübl, Eric Müller, Vitali Karasenko, Stephan Hartmann, Vasilis Thanasoulis, Johannes Partzsch Main topics: Bug in UDP-Core for Virtex5 Trigger over GPIO-Header of FPGA-Boards New systemtime trigger problem HICANN-PLL Highspeed-Init/frequence change problem HostARQ Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20131022	
2013-11-05 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: J. Partzsch, S. Hartmann, V. Thanasoulis, E. Müller, A. Grübl Main topics: Status of Kintex-Design Flow Control in the new UDP-Core Reworking the Virtex-Designfor new UDP-Core Pulsetest wirh HALBE and new system-time initialisation Adding Host-ARQ into Virtex-Design Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20131105	Video conference

Start Date	Subject	Description	Location
2013-11-05 16:00:00.0	SP9 JourFixe TelCo	SP9 JourFixe TelCo Participants: CNRS (phone), KTH (video), Manchester (video), EPFL (phone), Dresden (phone), Heidelberg (video), Fraunhofer (phone), Sabanci (video)	
2013-11-26 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: A. Grübl, V. Karasenko, V. Thanasoulis, J. Partzsch Main topics: Packet-definition for Host-FPGA communication Format of data for the Host-FPGA communication Integration host-ARQ into FPGA-Toplevel FPGA-Release Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20131126	Video conference
2013-12-03 16:00:00.0	SP9 JourFixe TelCo	JourFixe Video conference of the SP9 part. Participants: • CNRS (video): Andrew Davison and Irina Kopysova • FG (video) Oswin Ehrmann • KTH (video) Anders Lansner • POLITO (phone) Andrea Acquaviva (for Enrico Macii) • UHEI (video) Karlheinz Meier, Andreas Gruebl and Bjoern Kindler • UMAN (phone) David Lester • SU (video) Yasar Gurbuz • TUD (phone) Rene Schueffny	TelCo
2013-12-04 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: A. Grübl, E. Müller, A. Kononov, V. Thanasoulis, J. Partzsch Main topics: Host-ARQ Scope-trigger Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20131204	Video conference
2014-01-16 08:30:00.0	SP9 (Neuromorphic Computing) meeting in Gif-sur-Yvette (France)	Meeting of SP9 partners in Gif-sur-Yvette. The meeting-agenda is available at: https://flagship.kip.uni-heidelberg.de/jss/Ag?eMAt=29&SgD=x&eKn=nm9bt1 Participants: list in EMDESK	Gif-sur-Yvette
2014-01-21 14:00:00.0	SP9 NMPM1 Software Video Conference (CNRS-UNIC/TUD/UHEI)	Participants: Bernhard Vogginger, Christoph Koke, Dominik Schmidt, Eric Müller, Joël Chavas, Karsten Wendt, Matthias Ehrlich, Mitja Kleider, Paul Müller, Sebastian Schmitt Main topics: Mailing list for external users Migration to new flow - show stoppers (i.e., ESS-via-halbe?) Calibration status Buildability (robustness) Towards nightly tests on hardware Details: https://brainscales-r.kip.uni-	Video conference

Start Date	Subject	Description	Location
		heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140121	
2014-01-21 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: Johannes Partzsch, Andreas Grübl, Eric Müller Main topics: Tests with Preout hostARQ testbench Layer 2 communication Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140121	Video conference
2014-01-28 10:00:00.0	SP9 PCB planning meeting (UHEI / Sabanci) in Heidelberg	Physical meeting in Heidelberg to start the joint effort between Sabanci and UHEI in assembling and testing the second generation of the Wafer-Scale Integration systems. Main topics: Three possible test setups will be used to perform the necessary tests The Main-PCB test setup MPTS The HICANN-Wafer test setup HWTS The final test setup FTS Tests performed with the MPTS by Sabanki Tests performed with the HWTS by Sabanki Tests performed with the FTS in Heidelberg by TUD Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Summary_of_the_meeting_in_Heidelberg_from_28_till_29_January_2014	Heidelberg
2014-02-04 14:00:00.0	SP9 NMPM1 Software Video Conference (CNRS-UNIC/TUD/UHEI)	Participants: Bernhard Kaplan, Christoph Koke, Eric Müller, Joël Chavas, Kai Husmann, Karsten Wendt, Mitja Kleider, Paul Müller, Sebastian Schmitt Main topics: ESS users Current ESS Future ESS Executing automatic tests HBP SP9 Specification Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140204	Video conference
2014-02-04 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: ADC Trigger Spike Times - Verification Bit file compatibility? Flashen Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140204	Video conference

Start Date	Subject	Description	Location
2014-02-04 16:00:00.0	SP9 JourFixe TelCo	Videoconference (JourFixe) of the SP9 project. Participants: CNRS (phone): Andrew Davison KTH (phone) Mikael Djurfeldt (for Erwin Laure) POLITO (phone) Andrea Acquaviva (for Enrico Macii) + Gianvito Urgese UHEI (video) Karlheinz Meier, Bjoern Kindler UMAN (video) Steve Furber SU (video) Yasar Gurbuz + Volkan Özgüz TUD (phone) Rene Schueffny and Sebastian Hoeppner	TelCo
2014-02-11 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: More of the HICANN configuration packets could/should be sent via the FPGA playback memory Current limit of playback pulses 2 FPGA boards in Heidelberg problems hostARQ integration Scope trigger pin Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140211	Video conference
2014-02-18 14:00:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Repo dependencies Automated (HW) Tests Providing Calibtic, StHAL, ... (master branches) to calibrators/local users Docker Image Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140218	Video conference
2014-03-04 16:00:00.0	HBP SP9 JourFixe Meeting	Monthly SP9 planning meeting. Attendants: • CNRS (video): Andrew Davison and Joel Chavas • KTH (phone) Mikael Djurfeldt (for Erwin Laure) • FhG (video): Oswin Ehrmann • SAP (phone) Frank Gottfried • UHEI (video) Karlheinz Meier, Bjoern Kindler • UMAN (video) Steve Furber and David Lester • SU (video) Yasar Gurbuz + Volkan Özgüz • TUD (phone) Rene Schueffny + Agenda: Approval of the minutes.pdf from 4 February 2014 Round table: report from all SP9 groups Follow-ups from the TelCo on 4 February 2014 Status of the specification document, in particular also the KPI (key performance indicators). Planning of the Sabanci meeting (10 April 2014) AOB	TelCo

Start Date	Subject	Description	Location
2014-03-17 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main Topic: Short status report of UHEI and SU status on PCB and system development Start planning for SU test PCB development. URL: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Mar_17_2014	Video conference
2014-03-18 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: E. Müller, V. Karasenko, A. Kononov, A. Grübl, J. Partzsch, S. Hartmann, S. Scholze, V. Thanasoulis Main topics: Replacement of UDP-Core in the current FPGA by OpenCores UDP-Core discussion Test Kintex-Boards availability Replacement of Background Generators discussion FPGA hangs after experiment restart Failing L2 loopback tests (issue 1279) HostARQ-Implementation HICANN-ARQ Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140318	Video conference
2014-03-25 14:00:00.0	SP9 NMPM1 Software Video Conference (CNRS-UNIC/TUD/UHEI)	Main topics: Technical ESS discussion Docker PyHAL 0.7 to 0.8 conversion ESS users Status Updates Software Flows Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140325	Video conference
2014-03-25 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: A. Kononov, J. Partzsch, E. Müller, V. Karasenko Main topics: FPGA freezes hostARQ integration HALbe tests for L2 initialisation Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140325	Video conference
2014-04-01 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main topic: Discussion of FCTB's first version block schematic Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Apr_01_2014	Video conference

Start Date	Subject	Description	Location
2014-04-01 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: hostARQ tests Layer2 init Routing logic Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140401	Video conference
2014-04-15 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: E. Müller, V. Karasenko, M. Kleider, J. Partzsch, V. Thanasoulis, A. Grübl Main topics: HostARQ Experiment workflow Main-PCB and wafer-module: status / planning Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140415	Video conference
2014-04-28 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main Topics Discussion of test circuits Schematic suggestion / current measurements on single HICANNs to set appropriate resistances Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Apr_28_2014	Video conference
2014-04-29 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: J. Partzsch, V. Thanasoulis, E. Müller, V. Karasenko, A. Grübl Main topics: Flow-control Status of Kintex-design Status of Kintex-board production New ARQ-software in the test-bench Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140429	
2014-05-02 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main Topic SU presented corrected test circuits as a result of previous meeting More details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_May_02_2014	Video conference

Start Date	Subject	Description	Location
2014-05-06 14:00:00.0	SP9 NMPM1 Software Video Conference (CNRS-UNIC/TUD/UHEI)	Main topics: ESS questions Synapse loss over 30 % for only small number of neurons on small setup Synapse loss much higher for synapses from Spike Sources than for recurrent synapses Docker-based ESS distribution Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140506	Video conference
2014-05-06 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Status of Kintex-board production Flow-Control in the Phy Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140506	
2014-05-13 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: Eric Müller, Vitali Karasenko, Sebastian Höppner, Johannes Partzsch Main topic: Status of HostARQ Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140513	Video conference
2014-05-22 14:00:00.0	SP9 NMPM1 Software Video Conferences (CNRS-UNIC/TUD/UHEI)	Participants Christoph Koke, Constantin Pape, Eric Müller, Kai Husmann, Paul Müller, Sebastian Jeltsch, Sebastian Schmit, Bernhard Vogginger, Karsten Wendt, Matthias Ehrlich, Joël Chavas Main topics: PyNN-based tests for the ESS Towards PyHAL 0.8 ESS-specific tests Status of new flow: Marocco Details: https://brainscales-r.kip.uni-heidelberg.de/projects/symap2ic/wiki/Symap2icMeetingLog_20140522	Video conference
2014-05-27 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main topics: Corrected test circuits have been implemented into schematic (1 connector only) by SU Differential connections ok Reset and FPGA Power switch signals not yet correctly wired. Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_May_27_2014	Video conference

Start Date	Subject	Description	Location
2014-05-27 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Kintex7-order for HBP hostARQ-simulation hostARQ-tests and pulsdata hostARQ for Kintex7 Mannheim/Extoll Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140527	Video conference
2014-06-03 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: E. Müller, V. Karasenko, J. Partzsch, A. Grübl, Christian Leibig, Sebastian Höppner, S. Schiefer Main topics: Extoll-evaluation and Kintex integration HBP purchases HostARQ simulation Kintex7 integration Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140603	Video conference
2014-06-05 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main topics: Discussion of first complete version of FCTB schematic Connectivity of sample_trigger and ucd_reset_adc Layout comments Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Jun_05_2014	Video conference
2014-06-17 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: HostARQ tests on Virtex5 HostARQ on Kintex7 Status-/Debug-module in FPGA Kintex7 PCB production Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140617	Video conference
2014-06-24 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Preparation of the ISC2014 presentation/demonstration by Stephan Hartmann (invited by AVNET/Xilinx) Formatting of the Host-FPGA-data Puls-loopback-tests Blocking of reads via hostARQ Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140624	Video conference

Start Date	Subject	Description	Location
2014-07-01 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: UHEI-KIP: Eric Müller, Vitali Karasenko, Paul Müller, Andreas Grübl, UHEI-ZITI: Christian Leibig, Fynn Beuttenmüller, TUD: Johannes Parzsch, Vasilis Thanasoulis Main topics: Hardware tests Configuration read commands stability Simulation with 100k pulses showed missing pulses ExToll dd3 memory adapter for the kintex7 Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140701	Video conference
2014-07-11 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main topics: Two bugs in FCTB design regarding connector positions and pinout. Schematic approval for final layout. Add test and debug features to the board Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Jul_11_2014	Video conference
2014-07-14 15:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: Maurice Guettler, Dan Husmann, Andreas Grübl, Omer Ceylan, Melik Yazici Main topics: Pin-swap error in the FCTB connector pinout. FCTB design sign off for production Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Jul_14_2014	Video conference
2014-07-15 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Kintex7 HostARQ Virtex5 HICANN reads Virtex5 puls loopback Simulation with 8 HICANNs and HICANN-BEGs Simulation of the routing-logic Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140715	Video conference
2014-07-22 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Kintex7-Setup will be shipped to Heidelberg HICANN-ARQ-Simulation problem Kintex7-toplevel hostARQ-simulation Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140722	Video conference

Start Date	Subject	Description	Location
2014-07-29 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Issues with simulation of tm_arqburnin State of Kintex 7 design Problems with design stability Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140729	Video conference
2014-08-04 09:00:00.0	SP9: TelCo regarding the planned demo of the job submission to the NM platforms	Discussion with UHEI (NM-PM1), Manchester (NM-MC1), CNRS-UNIC (web-component), EPFL (Unified Portal / user authentication)	Tele-conference
2014-08-05 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Participants: Eric Müller, Vitali Karasenko, Johannes Partzsch Main topics: Timing ARP Behaviour HICANN Reads SendUDP JTAG Kintex Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140805	Video conference
2014-08-12 15:30:00.0	SP9 NMPM1 FPGA Firmware Video Conferences (TUD/UHEI)	Main topics: Stability of current design with packets from own or foreign subnets HICANN-Read Problematik Neues ETH-Stim Stand Kintex7 Design Details: https://brainscales-r.kip.uni-heidelberg.de/projects/hmf-fpga/wiki/FPGAMeetingLog_20140812	Video conference
2014-08-15 14:00:00.0	SP9 PCB planning video conference (UHEI / Sabanci)	Participants: SU: Yasar Gurbuz, Melik Yazici, UHEI: Dan Husmann, Andreas Grübl Main topics: Planning of Wafer Assembly Training in Heidelberg Rough Schedule for MainPCB production. Details: https://brainscales-r.kip.uni-heidelberg.de/projects/pcb-wsiv2/wiki/Notes_of_vidco_on_Aug_15_2014	Video conference
2014-09-01 14:00:00.0	SP9 Job-Queue-Demo meeting	Video conference UHEI - UNIMAN - CNRS-UNIC - EPFL regarding the planned demo of the job queue interface to the neuromorphic computing platform. The demo is planned to be show in the HBP Summit meeting plenary session.	Video conference

Start Date	Subject	Description	Location
2014-09-10 14:00:00.0	SP9-SP6 Job-Queue-Demo meeting	Preparation meeting for demo of Neuromorphic platform at the HBP Summit. Participants CNRS-UNIC, UHEI, UMAN, EPFL	Video conference
2014-09-23 09:00:00.0	SP9 NM-PM1 System Assembly and Testing Workshop	Meeting with SU people Meeting Agenda: https://flagship.kip.uni-heidelberg.de/internal/jss/Ag?m=showAgenda&meetingID=47	Heidelberg

Annex E: HBP Meetings

Start Date	Subject	Description	Location
2014-04-10 09:00:00.0	HBP SP9/SP11.3 In-Person-Meeting in Sabanci (Turkey)	HBP SP9 planning meeting in Sabanci (Turkey) List of participants in EMDESK	Sabanci, Turkey
2014-05-06 16:00:00.0	SP9/SP11.3 JourFixe TelCo	Participants: • CNRS (video): Andrew Davison and Joel Chavas • EPFL (phone): Yusuf Leblebici and Tugba Demirci • FhG (phone): Oswin Ehrmann • KTH (phone): Anders Lansner and Erwin Laure • POLITO (phone): Andrea Acquaviva, Massimo Poncino and Andrea Calimera for Enrico Macii • SAP (phone) Frank Gottfried • SU (video) Yasar Gurbuz • TUD (phone) Sebastian Hoeppner • UHEI (video) Karlheinz Meier, Johannes Schemmel, Bjoern Kindler • UMAN (phone) Steve Furber • CSIC (video): Bernabe Linares-Barranco • UoS (phone): Michael Schmucker • UNIBI (video): Ulrich Rueckert	Video conference
2014-06-03 16:00:00.0	SP9/SP11.3 JourFixe TelCo	Participants: • CNRS (video): Andrew Davison and Joel Chavas • EPFL (phone): Yusuf Leblebici and Tugba Demirci • FhG (video): Oswin Ehrmann • KTH (video): Anders Lansner and Mikael Djurfeldt (for Erwin Laure) • POLITO (phone): Gianvito Urgese for Enrico Macii • SU (video) Yasar Gurbuz + Volkan Özgüz • TUD (phone) Sebastian Hoeppner and Rene Schueffny • UHEI (video) Karlheinz Meier , Johannes Schemmel, Bjoern Kindler • UMAN (phone) Simon Davison for Steve Furber • CSIC (phone - Australia): Bernabe Linares-Barranco • UoS (phone): Michael Schmucker • MU (phone): Chris Huyck • UNIBI (video): Ulrich Rueckert	TelCo
2014-06-16 18:30:00.0	HBP SP6 & SP9 Meeting	A cross-subproject meeting to discuss interactions between the Unified Portal (SP6) and Neuromorphic Platform (SP9). Agenda: Status of central authentication system Plans for model simplification tasks	Video-conference

Start Date	Subject	Description	Location
2014-06-24 14:00:00.0	Workshop: Super-computing & Human Brain Project? Following Brain Research & ICT on 10-Year Quest (HBP SP6, SP7, SP9 & SP13)	A workshop (Supercomputing & Human Brain Project – Following Brain Research & ICT on 10-Year Quest) was organised at the International Supercomputing Conference in Leipzig, Germany (22-26 June). The event was chaired by Thomas Schulthess (SP7 & SP13) and presentations were given by Thomas Lippert (SP7 & SP13), Felix Schürmann (SP6 & SP7), Markus Diesmann (SP6) and David Lester (SP9).	Leipzig, Germany
2014-07-17 09:00:00.0	HBP cross SP data / services video conference (SP1, SP2, P3, SP4, SP5, SP6, SP7, SP8, SP9, SP10, SP11)	Videoconference for all SPs regarding their data and data-service offers and needs. The agenda of the meeting and uploaded talks are available at: https://flagship.kip.uni-heidelberg.de/jss/Ag?eMAt=34&SgD=x&eKn=ExDtP2	Video conference
2014-07-24 09:00:00.0	SP9/SP11.3 in-person-meeting in Berlin	Full day quarterly physical meeting of the SP9 and SP11.3 participants in Berlin. Agenda attached in EMDESK. Uploaded talks on the SP9 internal server at: https://flagship.kip.uni-heidelberg.de/internal/jss/Ag?m=SgD&mI=3	
2014-08-05 16:00:00.0	SP9/SP11.3 JourFixe TelCo	Participants: • CSIC (phone): Bernabe Linares-Barranco • KTH (video): Mikael Djurfeldt (for Erwin Laure) • TUD (phone) Sebastian Hoeppner • UHEI (video) Karlheinz Meier, Johannes Schemmel, Björn Kindler • UMAN (video) Steve Furber and David Lester • UNIBI (phone): Ulrich Rueckert • UoS (video): Thomas Nowotny and Michael Schmucker	TelCo
2014-08-19 09:00:00.0	Collaboration SP-Meeting (SP1, SP5, SP7 & SP9)	'Modeling pyramidal neurons using neuromorphic technologies' Meeting Meeting attendees: Javier DeFelipe (UPM), Karlheinz Meier (UHEI), Ôscar Herreras (External collaborator, IC-CSIC); Luis Pastor (URJC); Gonzalo Leôn (UPM), members of the Cajal Cortical Circuits Laboratory; Spanish representatives of SP5 & SP7 (visualization)	Madrid (Spain)
2014-09-02 09:00:00.0	SP9 JourFixe TelCo	Representatives were present from: Heidelberg, Dresden, Manchester, Sabanci, KTH, Fraunhofer, CNRS, SESIC, Bielefeld, Sussex. Minutes attached in EMDESK	TelCo
2014-09-30 08:30:00.0	SP4, SP6 & SP9 Meeting at the HBP Summit	Cross-SP meeting; chaired by Karlheinz Meier	Heidelberg
2014-09-30 09:30:00.0	HBP SP6, SP7 & SP9 Meeting at the HBP Summit	Cross-SP meeting; chaired by Karlheinz Meier	Heidelberg

Annex F: External Meetings

Presentations have been part of a dissemination strategy to make the Human Brain Project—particularly its emphasis on ICT tools—known to different fields in academia and industry. Neuromorphic computing in the HBP is now internationally recognised as a key activity in the Project.

Start Date	Title	Location	Description	Partner
2013-10-04	Synthesizing Thought - Novel Computing Architectures for the Human Brain Project	Dublin	Talk at IEF2013	UHEI
2013-10-14	Neuromorphic Computing and the Human Brain Project	Heidelberg	Talk at flagship: Joined EU / US workshop on cortical processors	UHEI
2013-10-17	The EU Human Brain Project	Prague	Talk at Horizon2020 Konferenz/ TEERA2020	UHEI
2013-10-21	Physikalische Modelle des Gehirns - Technologien, Theorien und Synthese	Wuppertal	Festvortag zur Jubiläumsveranstaltung der UNI Wuppertal / Festkolloquium	UHEI
2013-10-24	Physical Models of the Brain - Technologies, Theories and Synthesis	Groningen	Talk / Physikalisches Kolloquium	UHEI
2013-10-25	Physical Models of the Brain - Technologies, Theories and Synthesis	Karlsruhe	Talk / Physikalisches Kolloquium	UHEI
2013-10-30	"How to simulate without a Computer - A Physics Approach to the Brain"	Hamburg	Jentschtke-Lecture am DESY	UHEI

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2013-11-09	Breaking the Wall of Traditional Computing / Untertitel: How the Human Brain Project can Contribute to a Fundamentally New Paradigm of Information Processing	Berlin	Talk at the Falling Walls Konferenz 2013	UHEI
2013-11-14	Physical Models of the Brain - Technologies, Theories and Synthesis	Siegen	Talk / Physikalisches Kolloquium	UHEI
2013-11-18	Physical Models of the Brain - Technologies, Theories and Synthesis	Darmstadt	Talk / EMMI Physics Days 2013	UHEI
2013-11-19	Neuromorphic cognitive systems: emerging technologies for brain-inspired-computation	Brüssel	Vortrag im FET Seminar neuromorphic computing	UHEI
2013-11-27	The European Human Brain Project? Synthesis from the Nanoscale Up	Venedig	Talk at NANOTECHITALY2013	UHEI
2013-12-10	The EU Human Brain Project	Heidelberg	Talk / Opening HBP Platform Heidelberg	UHEI
2013-12-16	The EU Human Brain Project	New York	Talk at the Inaugural Bioelectronic Medicines Summit / GSK	UHEI
Start Date	Title	Location	Description	Partner
2014-02-03	Das EU-Flagship Human Brain Project - eine Herausforderung für Physikerinnen und Physiker in Deutschland und Europa	Brussels	DPG Informationsveranstaltung/Gesprächskreis Brüssel	UHEI
2014-02-05	Neuromorphic analogue VLSI	KTH, Stockholm	Workshop	UHEI

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2014-02-07	"From Ions to Electrons - Physical Models of Brain Circuits "	INCF, Stockholm	INCF Seminar	UHEI
2014-02-16	Mimicking the brain for better computing HBP Session	Chicago	AAAS 2014 Annual Meeting	UHEI
2014-02-24		Sandia, USA	NICE Workshop	UHEI
2014-03-11	Human Brain Project	Lund University, Sweden	Colloquium	UHEI
2014-03-26	"From Theory to Devices and Architectures"	Paris	Talk at the EITN Opening	UHEI
2014-03-28	" From Ions to Electrons - Physical Models of Brain Circuits"	Grenoble	Colloquium, Institut Laue-Langevin (ILL)	UHEI
2014-04-12	Neurons to Cognitive Computing Systems	Ankara University Ankara Turkey	Invited Seminar at Brain Awareness Conference	SU
2014-04-22	Human Brain Project	Stuttgart	Talk at MWK, Stuttgart	UHEI
2014-04-25	From Ions to Electrons - Physical Models of Brain Circuits	Bonn, Germany	Colloquium, University Bonn	UHEI
2014-04-29	HBP - From Ions to Electrons - Physical Models of Brain Circuits	Kiel, Germany	Colloquium University Kiel	UHEI
2014-05-10	An Engineers Attempt to Understand the Brain	Üsküdar University, Istanbul	Invited Talk at Bioengineering and Genetics Days	SU
2014-05-19	From Ions to Electrons - Physical Models of Brain Circuits	Aachen, Germany	Colloquium RWTH Aachen	UHEI
2014-05-27	Human Brain Project	Paris	Keynote Talk at YRLS2014	UHEI
2014-05-29	Human Brain Project	Istanbul	Invited Talk at 12th National Neuroscience Conference	SU

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2014-05-30	Neurons to Evolving Computing Systems	Istanbul	Invited Talk at the 12th National Neuroscience Conference	SU
2014-06-04	Human Brain Project		Invited Talk at the H2020 National Launch Event	SU
2014-06-10	Synthesizing Thought - The European Human Brain Project	Antalya, Turkey	Talk, 5th US-Turkey Advanced Study Institute on Global Healthcare-Keynote	UHEI
2014-06-19	Neurons to Computing Systems	Kayseri, Turkey	Invited Seminar at 21st Statistical Physics Conference	SU
2014-06-19	The HBP Mixed Doubles: Computing for Neuroscience and Neuroscience for Computing	Tel Aviv	The 1st HBP Education Workshop on New Frontiers in Neuroscience and Methods of Transdisciplinary Education	UHEI
2014-06-23	Neurons to Computing Systems	Eskişehir, Turkey	Invited Talk at 22nd National Biology Conference	SU
2014-06-26	Human Brain Project	Berlin	Parlamentarisches Frühstück	UHEI
2014-06-26	Brain derived Computing beyond von Neumann Achievements and Challenges?	Leipzig	Keynote at ISC'14 Supercomputing Conference	UHEI
2014-07-10	The EU Human Brain Project - A systematic Path from Data to Synthesis	Peking	WCCI2014 Conference	UHEI
2014-07-22	Nanotechnologies and Human Brain	Bodrum, Turkey	Keynote Speech at the 31st International Physics Congress	SU
2014-08-09	Sci-Foo-Camp/Googleplex	Mountain View, CA	Sci-Foo-Camp/Googleplex	UHEI
2014-08-11	Neuromorphic Computing in the European Human Brain Project	San Diego	Talk at Qualcomm	UHEI
2014-08-16	From Ions to Electrons - Physical Models of Brain Circuits	Heidelberg	International Conference of Physics Students ICPS 2014	UHEI

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2014-08-26	Visit by a member of the German parliament	Heidelberg	Visit of the UHEI HBP Group by Patricia Lips, chair of the "Ausschuss für Bildung, Forschung und Technikfolgenabschätzung" of the German Parliament	UHEI
2014-09-19	Beyond von Neumann -Brain derived Computing	London	Talk at RE.WORK TECH Conference	UHEI